

Keystone 13.3" Schematics

Skylake-U / Kabylake-U

2016-11-22

REV : A00

DY : None Installed

WWAN: WWAN only Installed

NON WWAN: NON WWAN Installed

DS3: Support DS3 Installed

NON DS3: NON DS3 only Installed

<Core Design>



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A4

Document Number

Keystone 13.3"

Rev

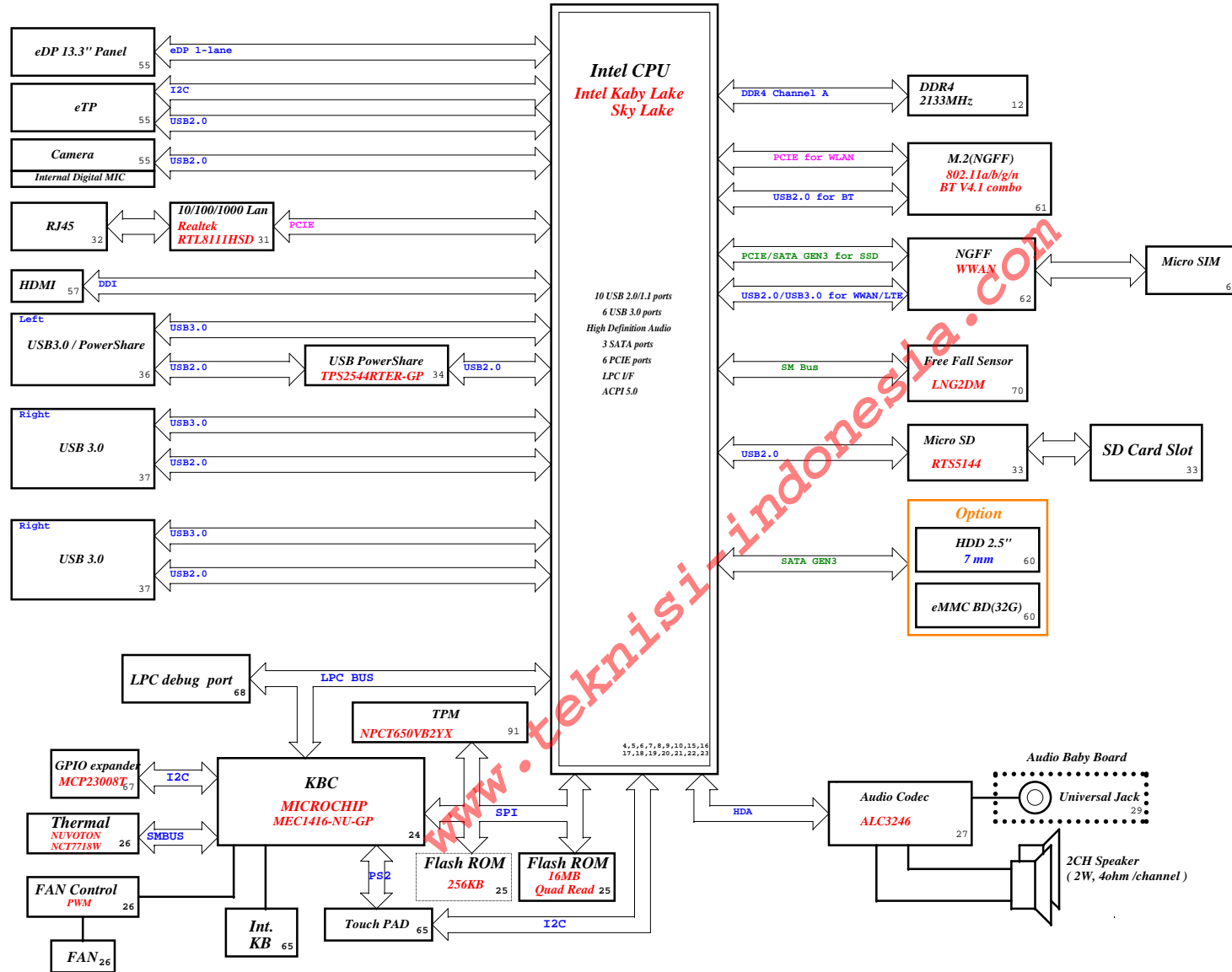
X00

Date: Wednesday, November 23, 2016

Sheet 1 of 106

Project code: 4PD0AW010001 (KBL)
Project code: 4PD0BH010001 (SKL)
PCB P/N: 16824
Revision: A00

Keystone 13.3" Block Diagram



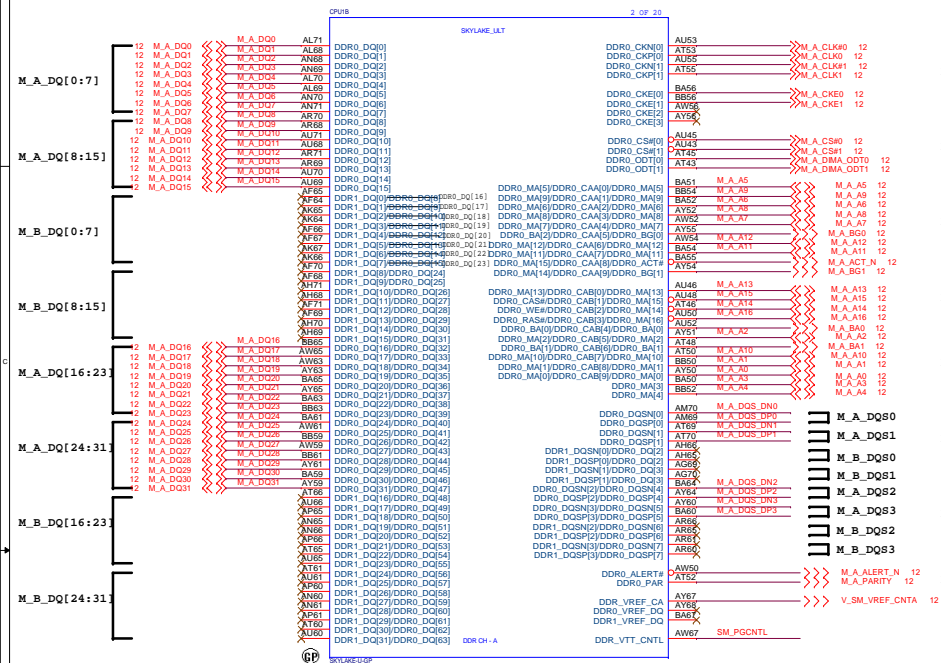
CHARGER		44
BQ24786RUYR		
INPUTS	OUTPUTS	
AD+	DCBATOUT	
BT+		
SYSTEM DC/DC		45
RT6575DGGW		
INPUTS	OUTPUTS	
	PWR 5V	
	5V_S5	
	5V_AUX_S5	
DCBATOUT		
CPU Core Power		46-50
NCP81218MNTXG		
NCP81381MNTXG		
NCP81381MNTXG		
NCP81253MNTBG		
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	
DCBATOUT	+VCCGT	
DCBATOUT	+VCCSA	
DDR4		51
RT8231AGQW		
INPUTS	OUTPUTS	
DCBATOUT	1D2V_S3	
	0D6V_S0	
CPU DCDC-V1D00A		52
AZ2261QI-10		
INPUTS	OUTPUTS	
DCBATOUT	1D0V_S5	
LDO-V1D8V		54
RT9025-25ZSP-2-GP		
INPUTS	OUTPUTS	
3D3V_S5	1D8V_S5	
LDO-V2D5V		54
RT9025-25ZSP-2-GP		
INPUTS	OUTPUTS	
3D3V_S5	2D5V_S3	
5V/3V S0		40
G5016KD1U		
INPUTS	OUTPUTS	
5V_S5	5V_S0	
3D3V_S5	3D3V_S0	
VCCSTG		40
APE8939GN3-GP		
INPUTS	OUTPUTS	
1D0V_S5	+VCCSTG	
VCCST		40
APE8939GN3-GP		
INPUTS	OUTPUTS	
1D0V_S5	+V1_00U_CPU	
SYSTEM DC/DC		45
RT6575DGGW		
INPUTS	OUTPUTS	
DCBATOUT	3D3V_AUX_S5	
	3D3V_S5	
	PWR 3D3V	

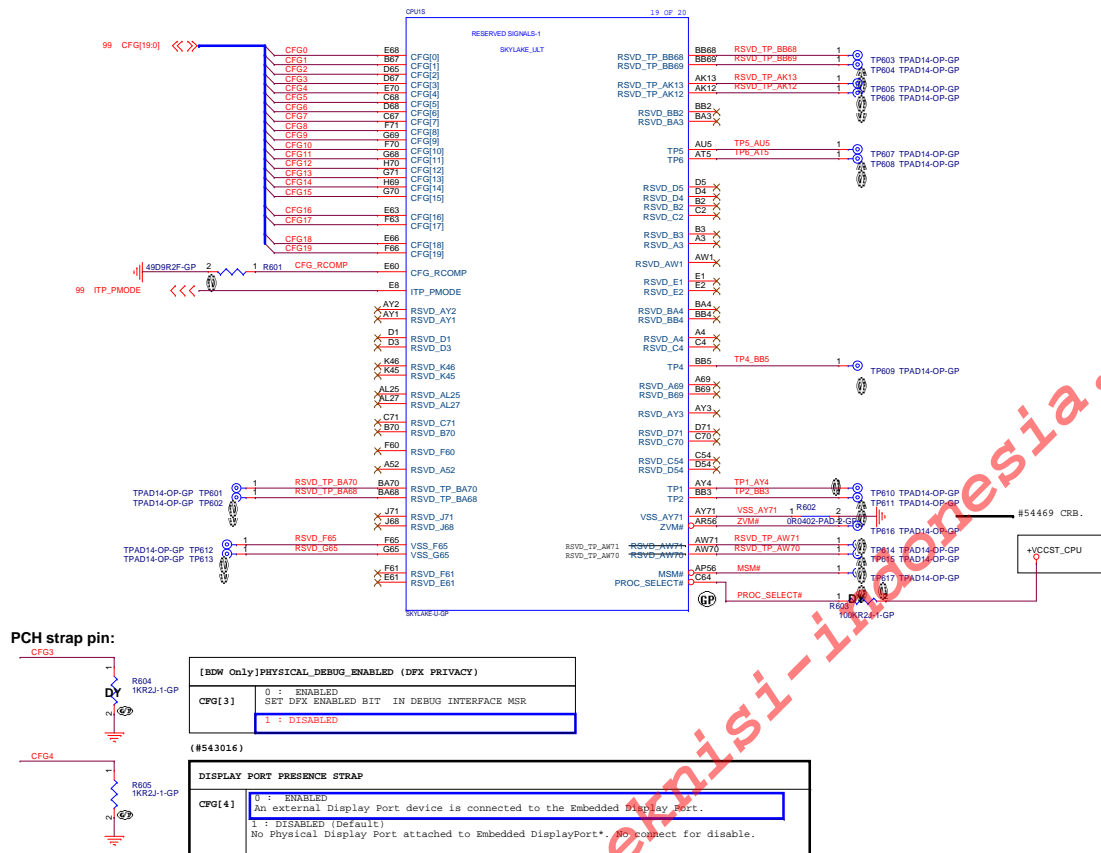
<Core Design>

Main Func = CPU

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SKL(#543016):

Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

<Core Design>

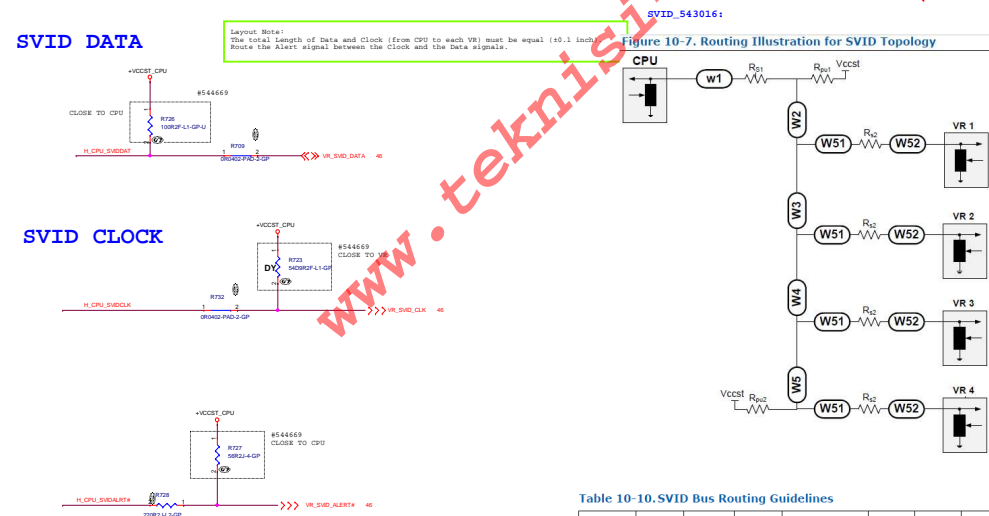
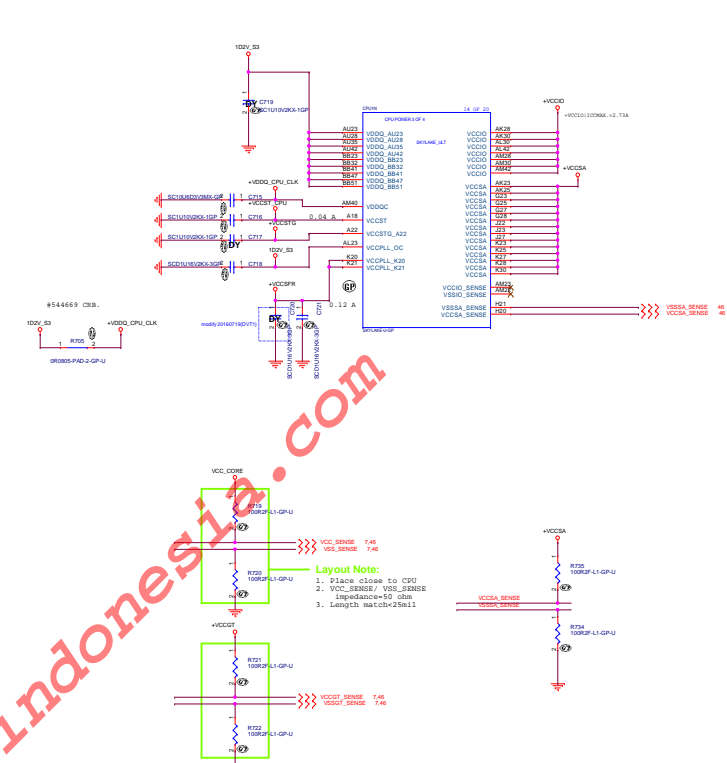
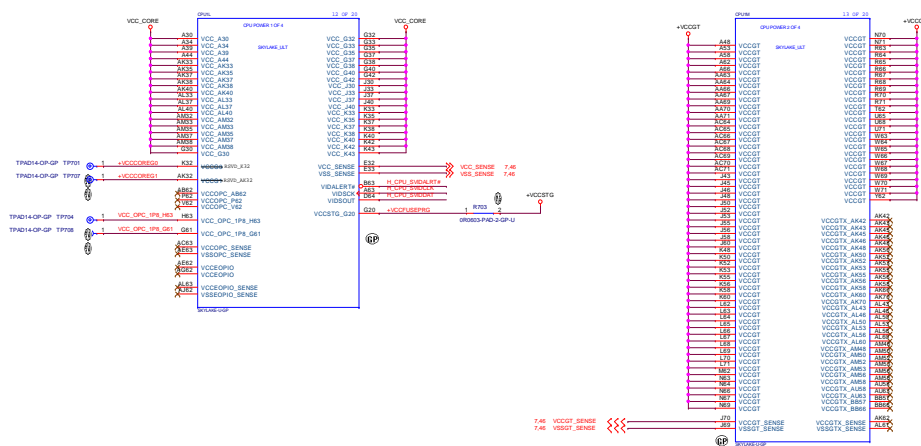
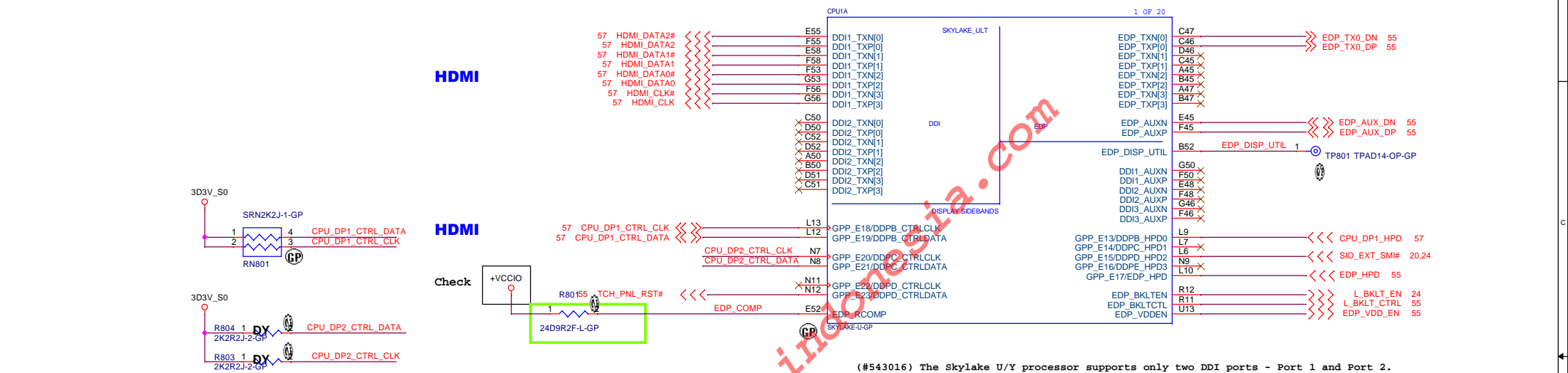


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R _{W1} [ft]	R _{W2} [ft]	R _{W3} [ft]	R _{W4} [ft]	R _{W5} [ft]	VCC ₁ [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10		1.0
VIDSCK							Empty	45	0	50		
VIDALERT #							56	Empty y	220	0		



(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω \pm 1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k \pm 5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k \pm 5% resistor	NC

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 Ω \pm 1% resistor.

Main Func = CPU

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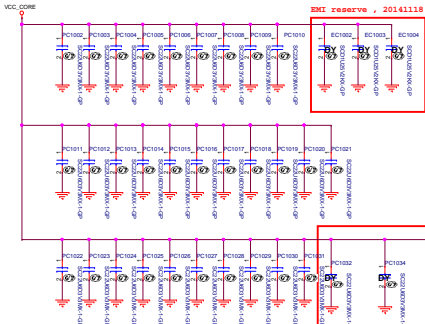
(#541016 PDS)

CORE

20140814 DAVID

U-line 23a 28W
IccMax current-I0wa max = 34 A

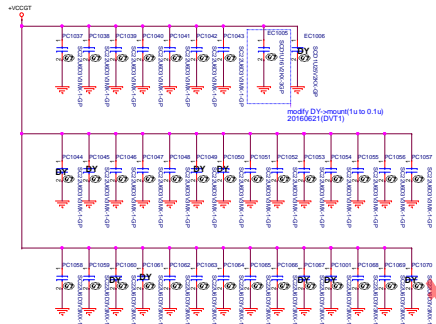
22U 0603 x 35(5 DV)



SLICED GT

U-line 23a 28W
IccMax current-I0wa max[A] = 67 A

22U 0603 x35 (5 DV)



VCCSA

22U 0603 x13 (4 DV)

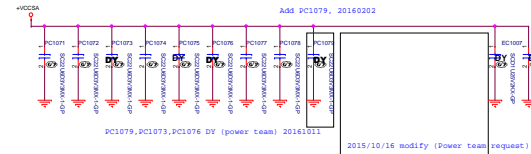


Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (04.5mO ESR)	Placed at primary side near to VR output
VCCGT Power Plane at VR output	1x 220uF (04.5mO ESR)	Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220uF (04.5mO ESR)	Placed at primary side near to VR output
VCCGTx Power Plane at VR output	1x 220uF (04.5mO ESR)	Placed at primary side near to VR output
VCCGTx Power Plane at VR output	1x 220uF (04.5mO ESR)	Additional components needed when supporting 23e
VCCIO Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

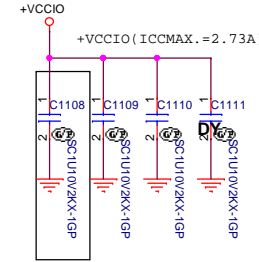
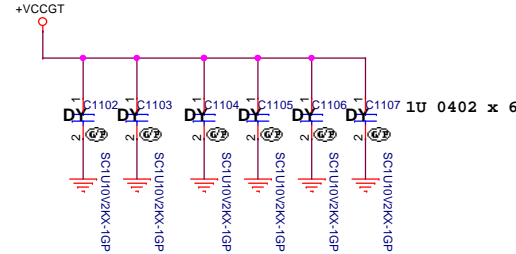
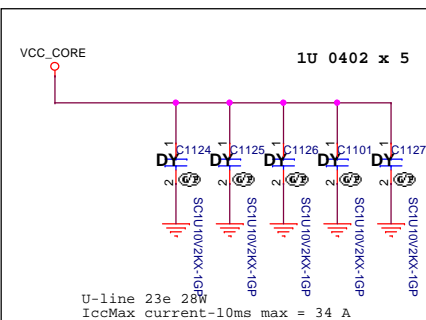
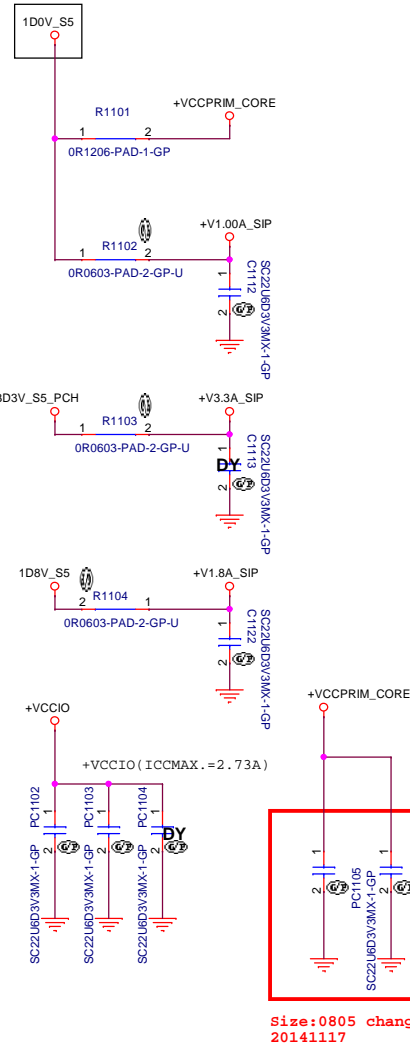
Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 220uF 0805		Place on secondary side, underneath the package
VCCGT	7x 10uF 0402		Place as close to the package as possible
VCCGTx	10x 10uF 0402		Place on secondary side, underneath the package
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPL	1x 1uF 0402		Place as close to the package as possible
VCCST	1x 1uF 0402		Place as close to the package as possible

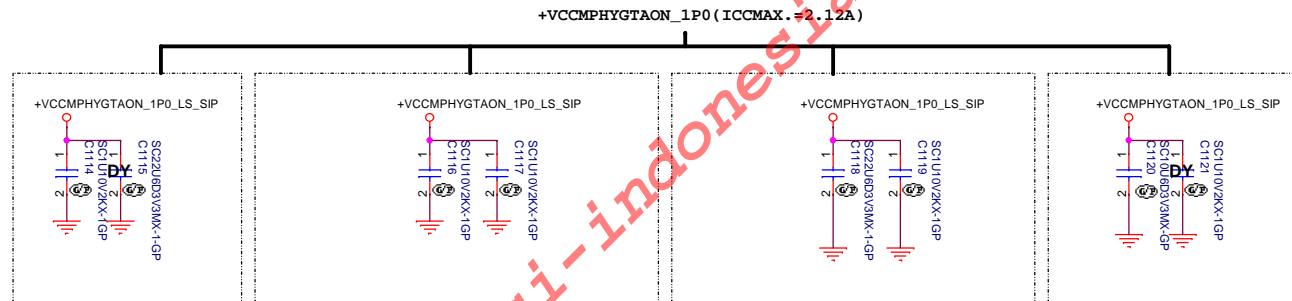
Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package
VCCSTG	2x 10uF 0402		Place on secondary side, underneath the package
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package
VCCSTG	6x 1uF 0201		Place on secondary side, underneath the package

VCCIO

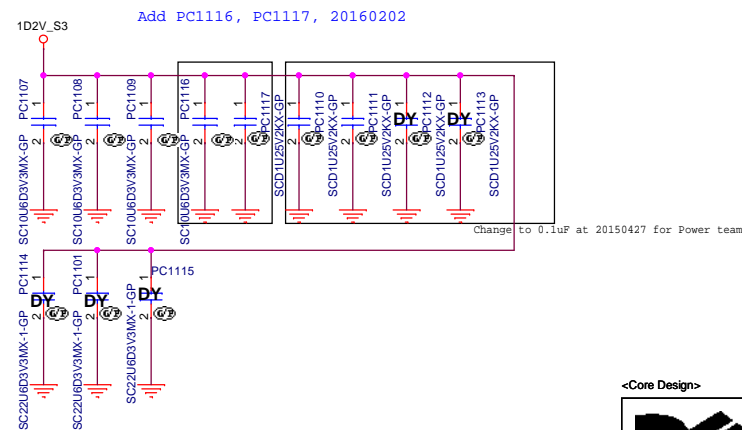


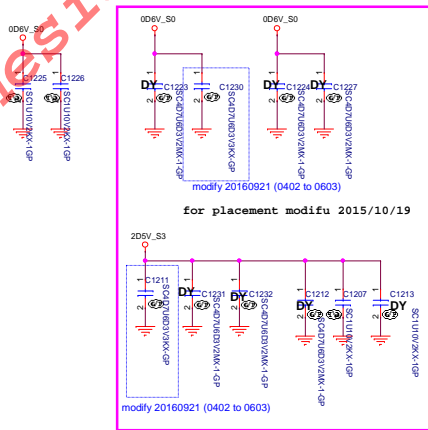
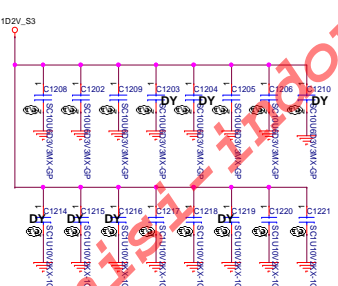
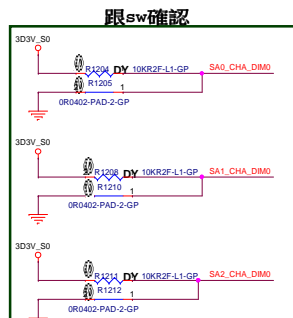
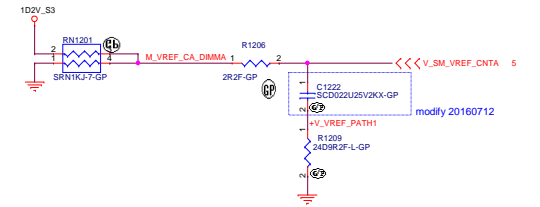
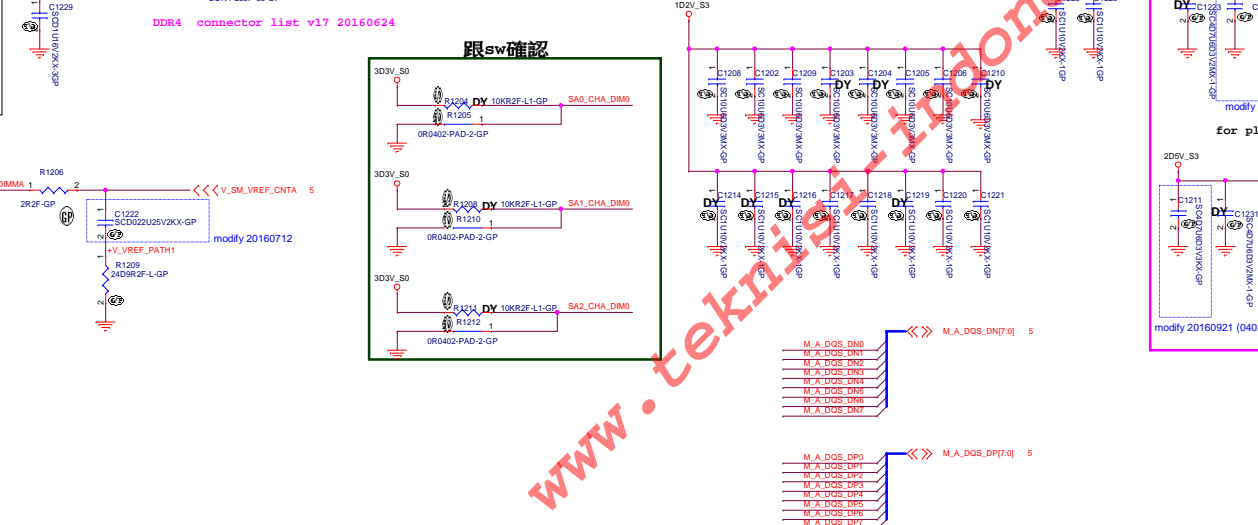
C1108 remove DY, 20160202



Layout Note:

1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15






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Title (Reserved)_SODIMM _SODIMM4					
Size A4		Document Number Keystone 13.3"			Rev X00
Date: Wednesday, November 23, 2016			Sheet 14 of 106		

Main Func = PCH

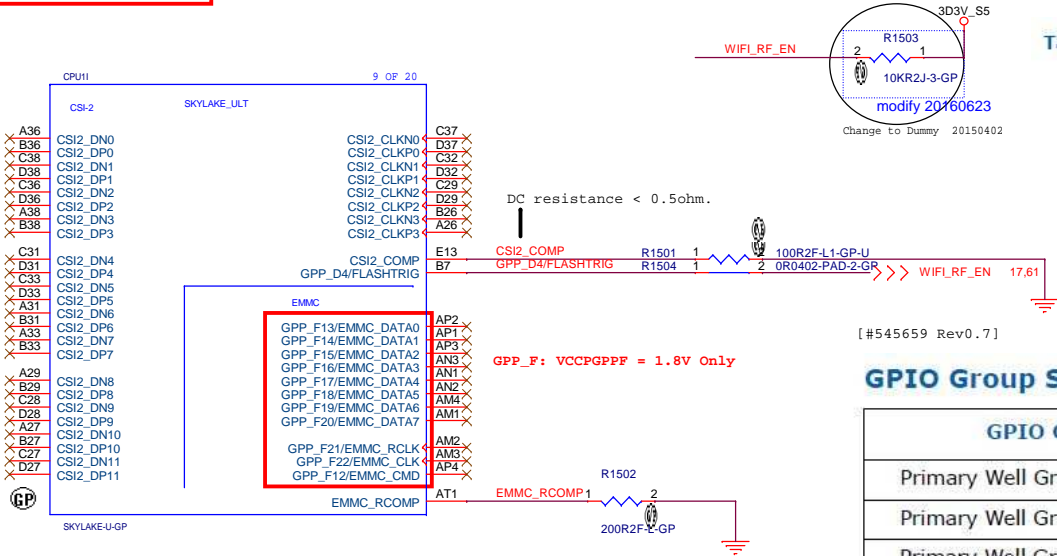


Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSENT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

Main Func = PCH

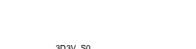
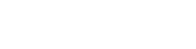
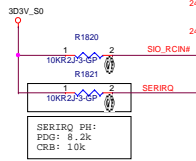
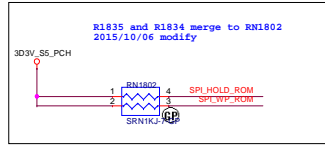
PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SMBALERT#/ GPP_CS	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC.

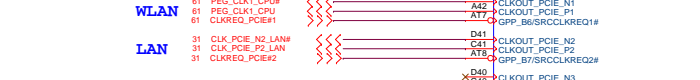
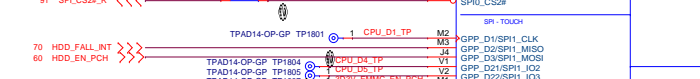
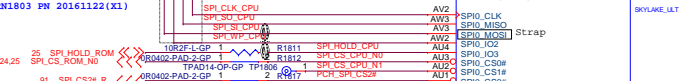
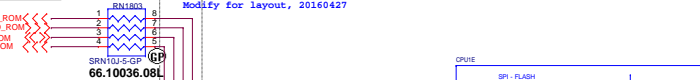
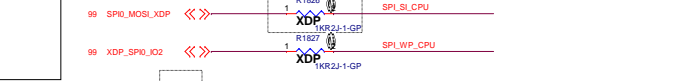
This signal has a weak internal pull-down.

PCH strap pin:

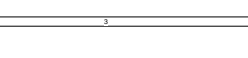
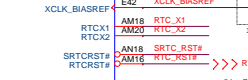
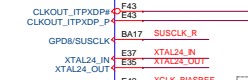
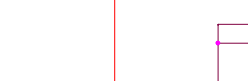
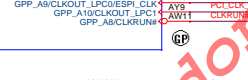
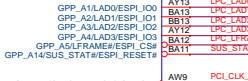
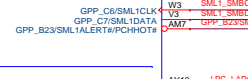
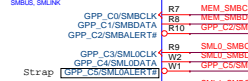
BOOT HALT	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU
SPI0_MOSI	This signal has a weak internal pull-up.



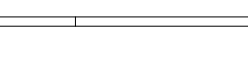
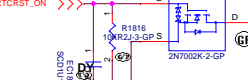
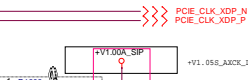
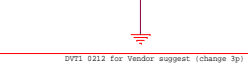
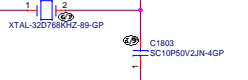
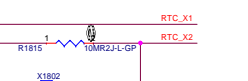
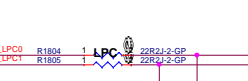
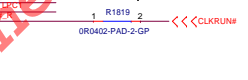
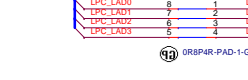
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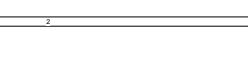
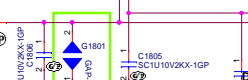
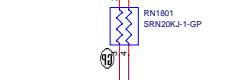
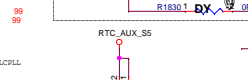
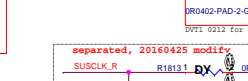
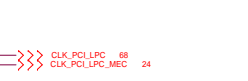
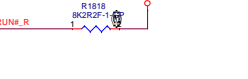
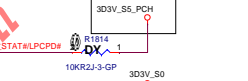
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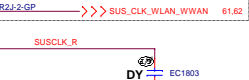
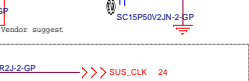
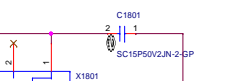
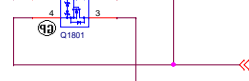
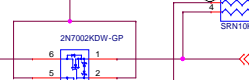
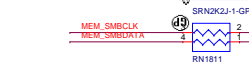
PLACE WITHIN 1.1 INCH OF PCH (#543016) Optional, can be left as OPEN/No-Connect.



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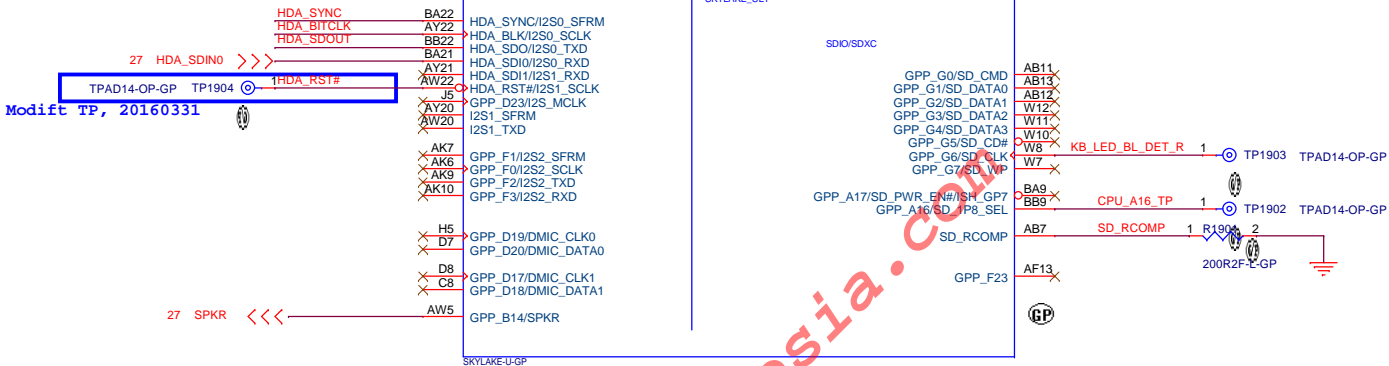


Main Func = PCH

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. ★ 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. ★ 1 = Port C is detected.

These two signals have weak internal pull-down.



PCH strap pin:

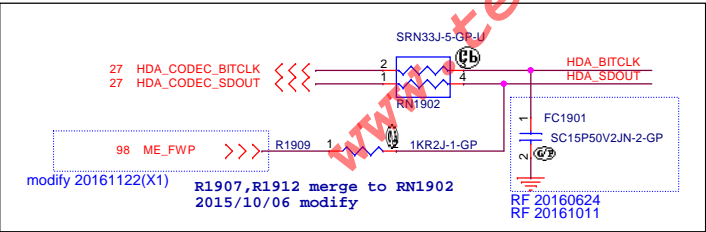
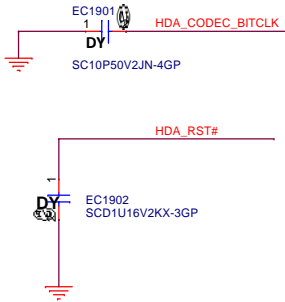
Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDO	Low = Default ★ High = Enable

The internal pull-down is disabled after PLTRST# deasserts

PCH strap pin:

NO REBOOT	
HDA_SPKR	★ Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts



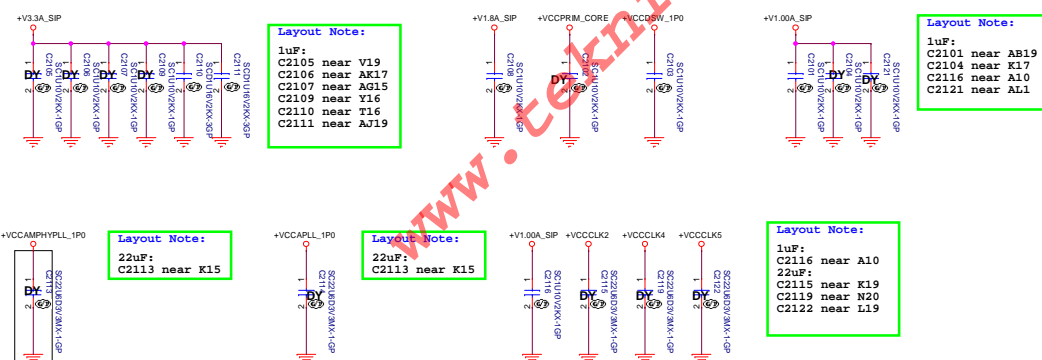
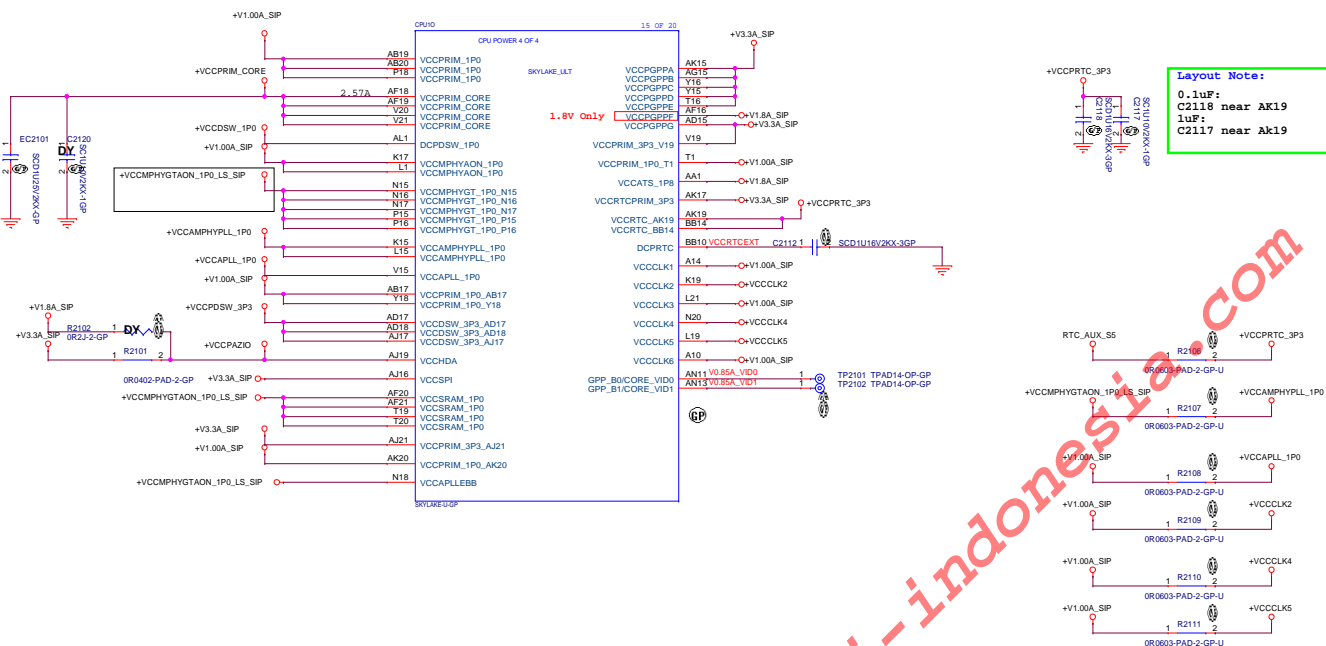
<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title
CPU (AUDIO/SDIO/SDXC)

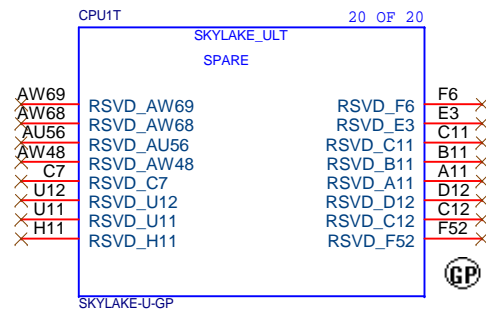
Size A3	Document Number Keystone 13.3"	Rev X00
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C2113 remove DY, 20160202

Main Func = PCH

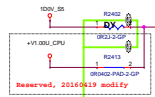


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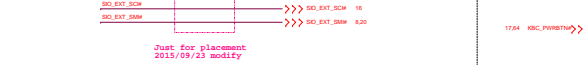
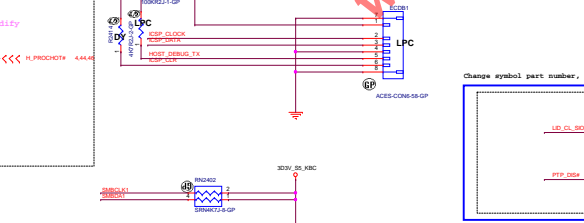
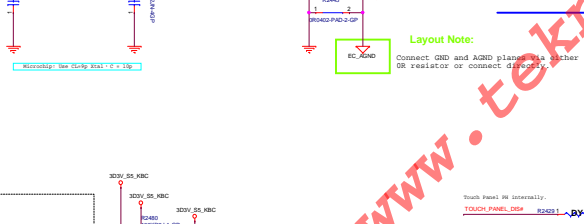
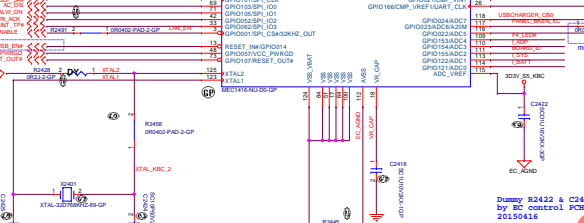
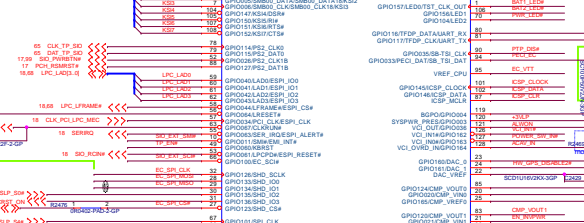
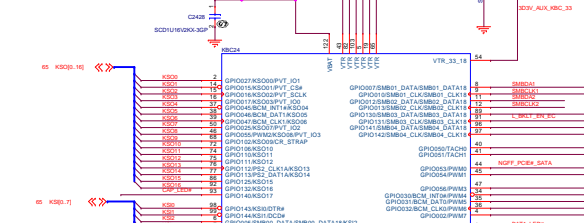
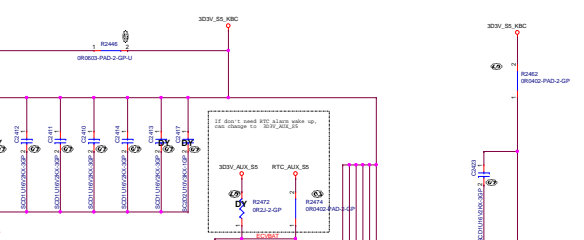
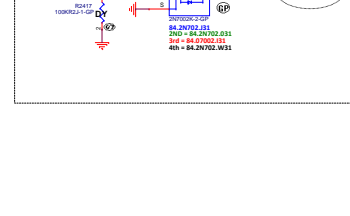
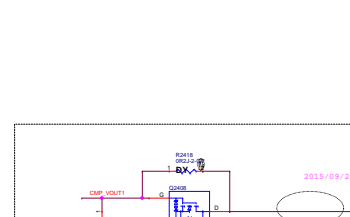
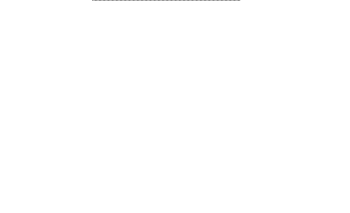
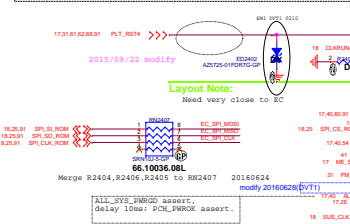
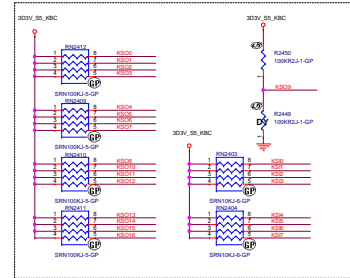
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CPU (RSVD)			
Size	Document Number		Rev
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Main Func = KBC

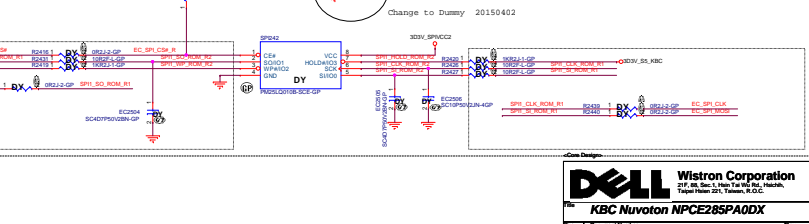
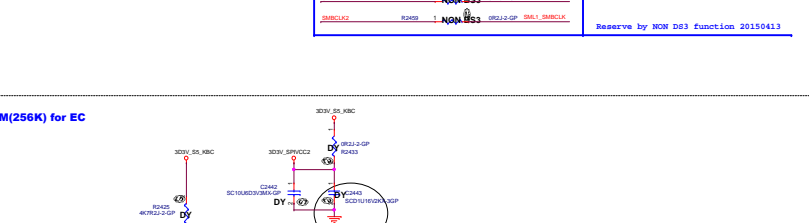
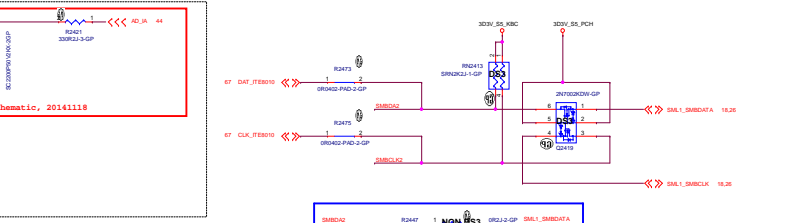
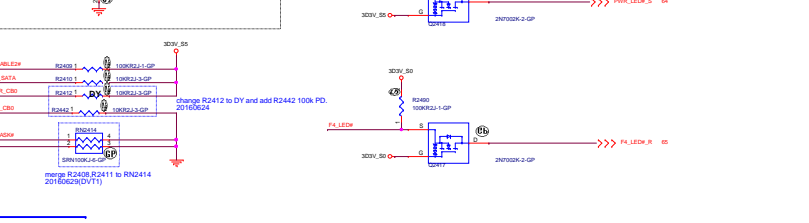
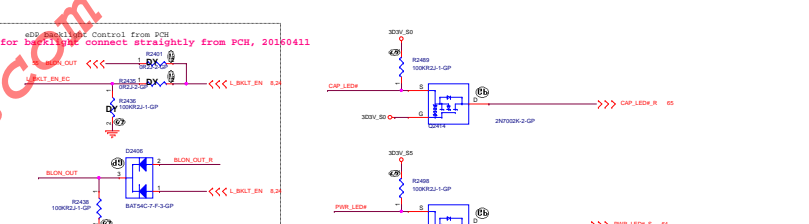
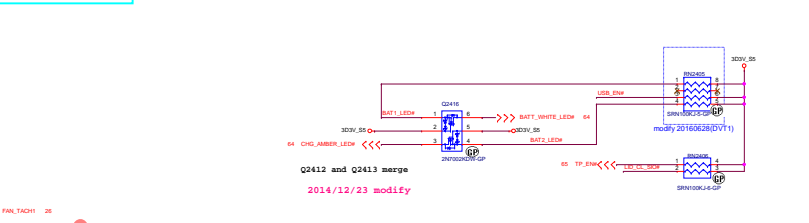
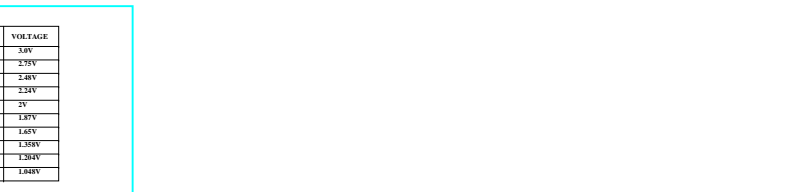
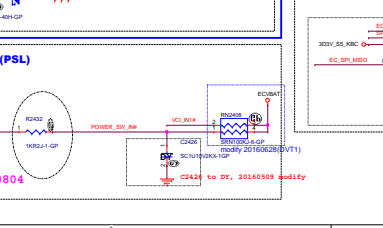
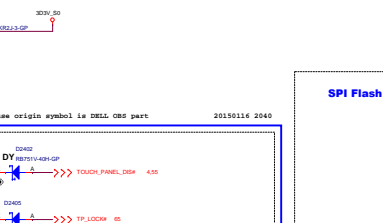
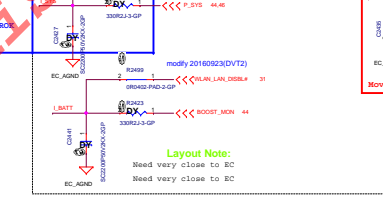
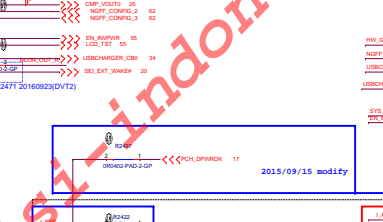
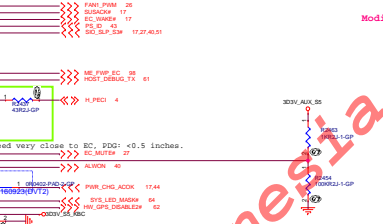
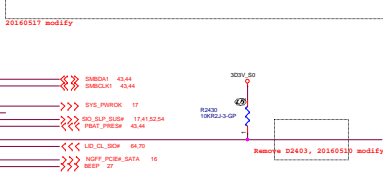


Layout Note:
Need very close to EC

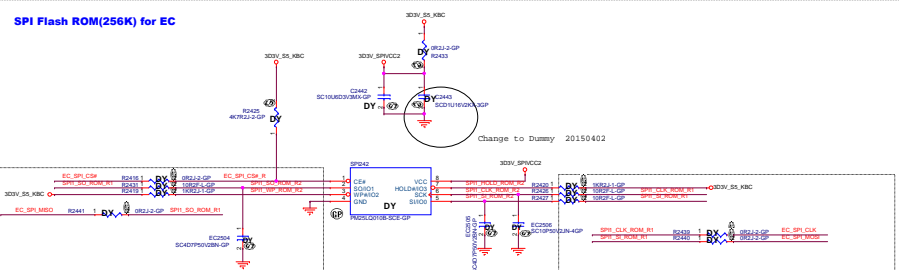
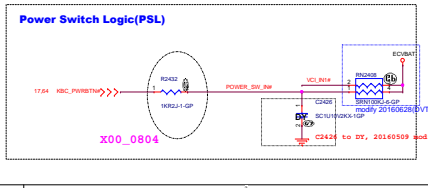
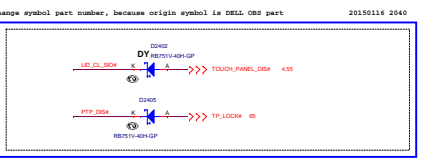


BOARD ID VERSION AD	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
TEVICA/TPM SKI	100K	20K	3.0V
TPVCA/TPM SKI	100K	20K	2.95V
DVT1 (SC) DVT1	100K	33K	2.40V
DVT2 (SC) DVT2	100K	47K	2.20V
X-build (1) A00	100K	75K	1.80V
	100K	100K	1.80V
	100K	174K	1.30V
	100K	215K	1.04V

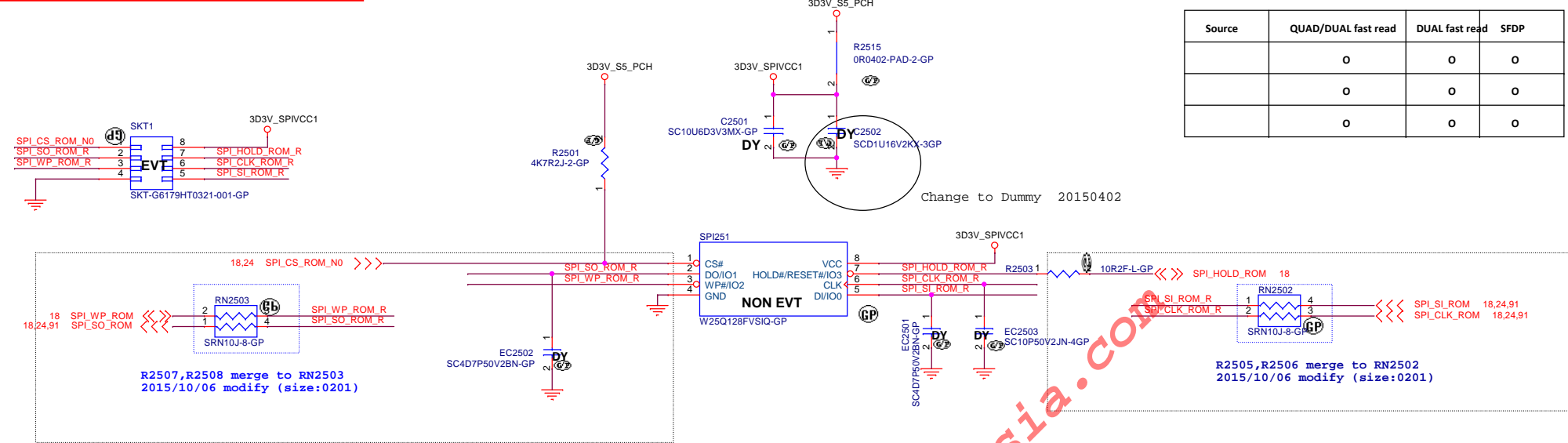
MEC1404 PN: 071.01404.0808 (KS13 Win schematics symbol)
MEC1406 PN: 071.01406.0006 (KS13 Win BOM)



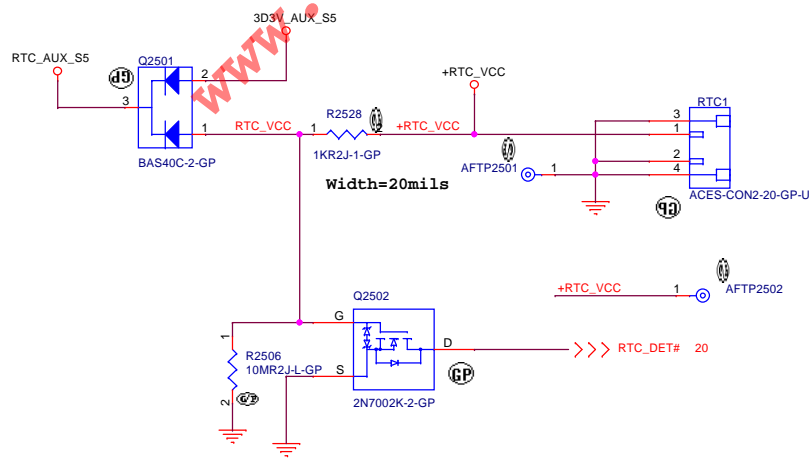
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Main Func = SPI Flash



Main Func = RTC



<Core Design>

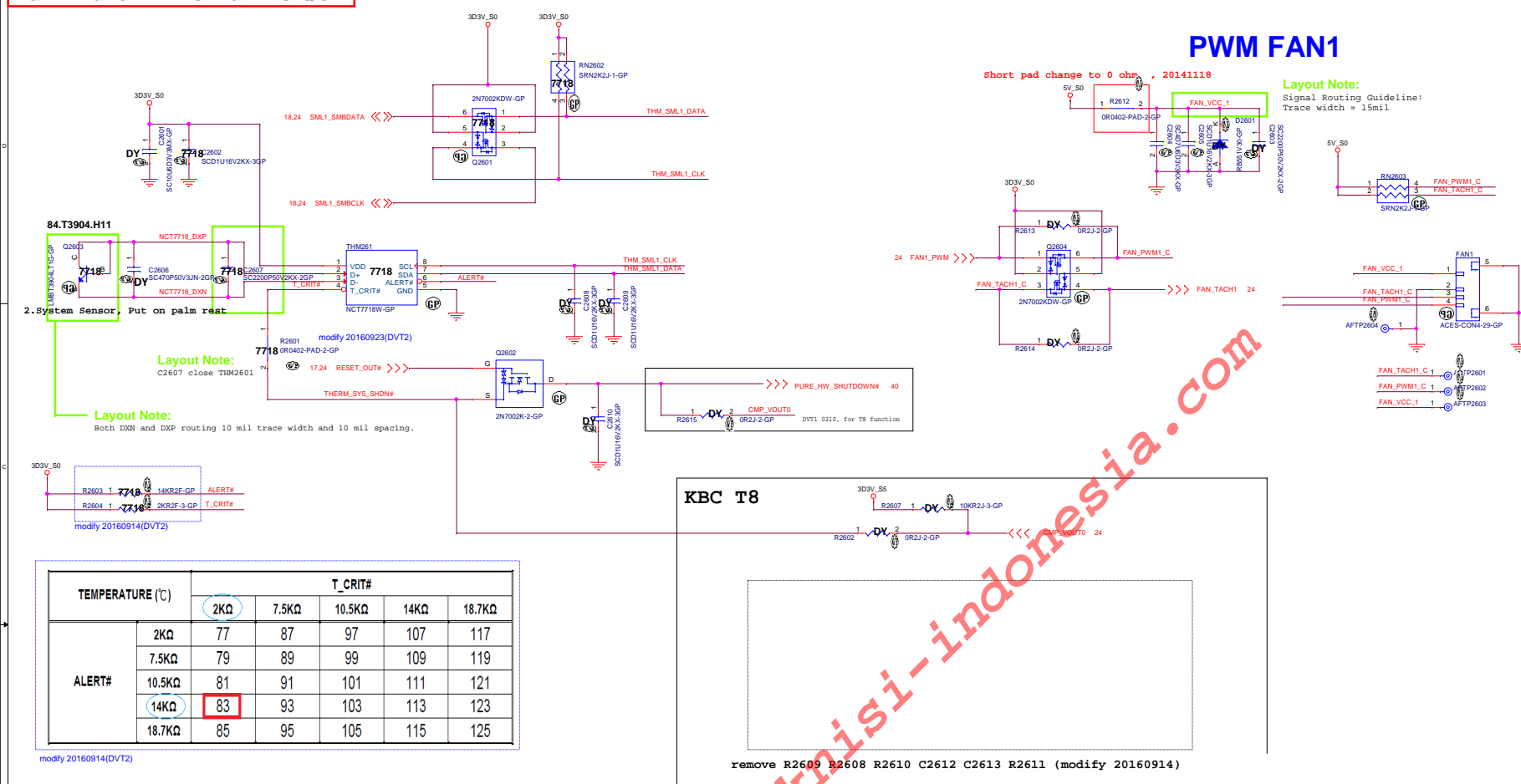
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Title
Flash/RTC

Size A3 Document Number
Keystone 13.3"

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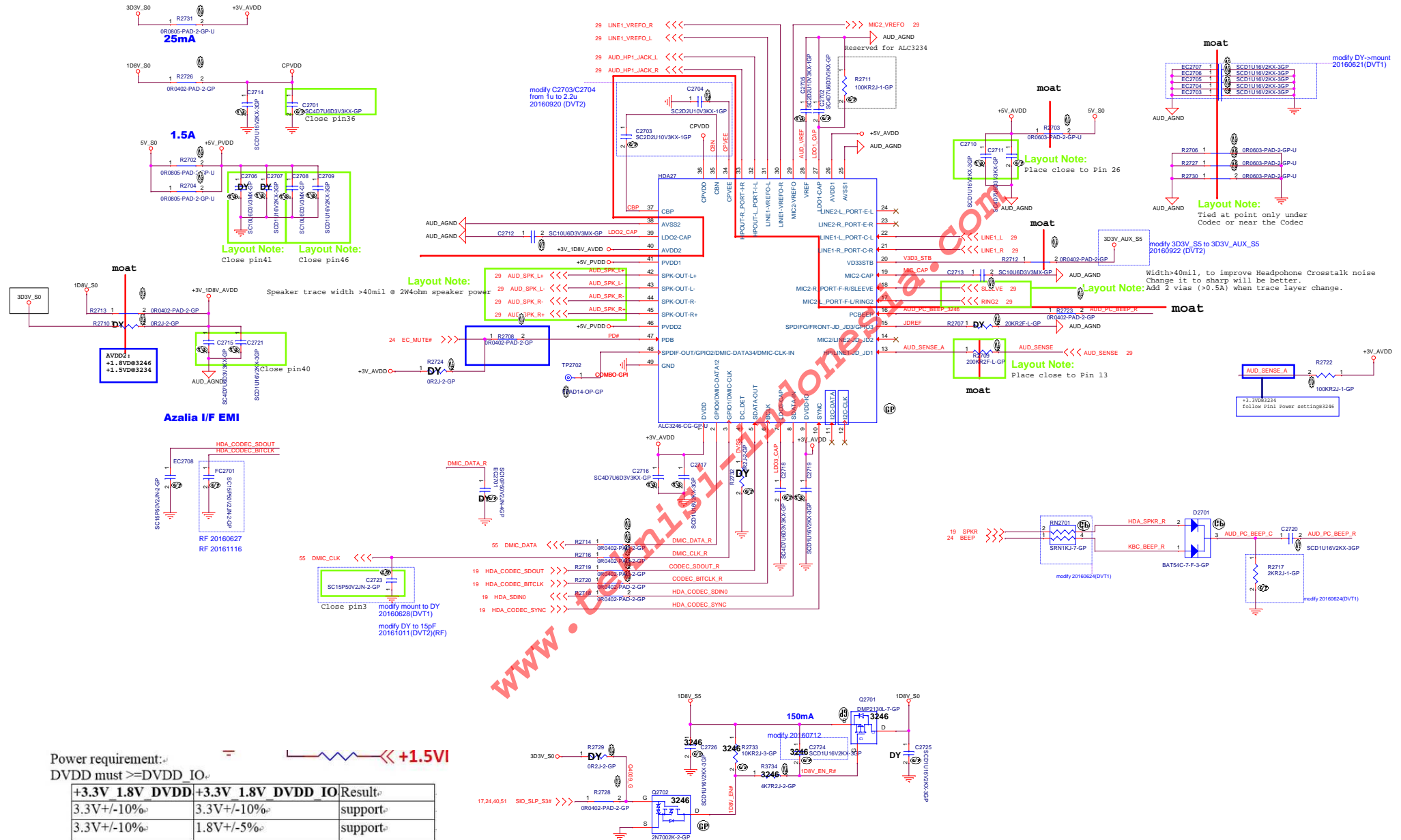
Rev
X00



TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

modify 20160914(DVT2)

Audio Codec Chip (ALC3246)



Power requirement:

DVDD must \geq DVDD_IO.

+3.3V 1.8V DVDD	+3.3V 1.8V DVDD IO	Result
3.3V+/-10%	3.3V+/-10%	support
3.3V+/-10%	1.8V+/-5%	support
1.8V+/-5%	1.8V+/-5%	support
1.8V+/-5%	1.5V+/-5%	support
1.8V+/-5%	3.3V+/-10%	Not support

◀Core Design▶

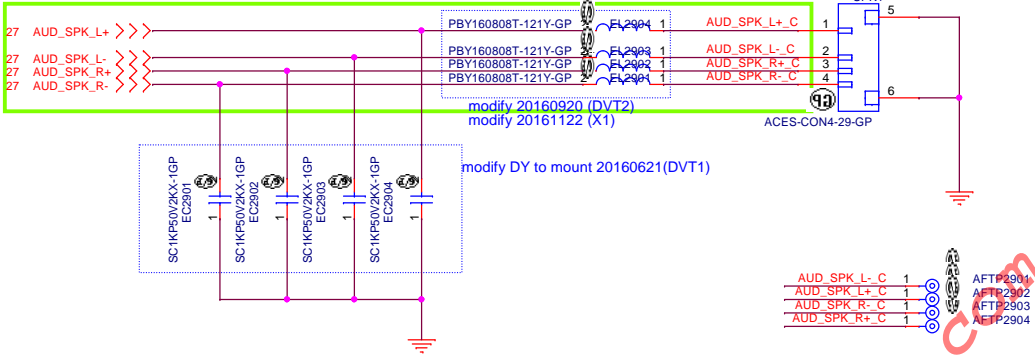
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Main Func = Audio

Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

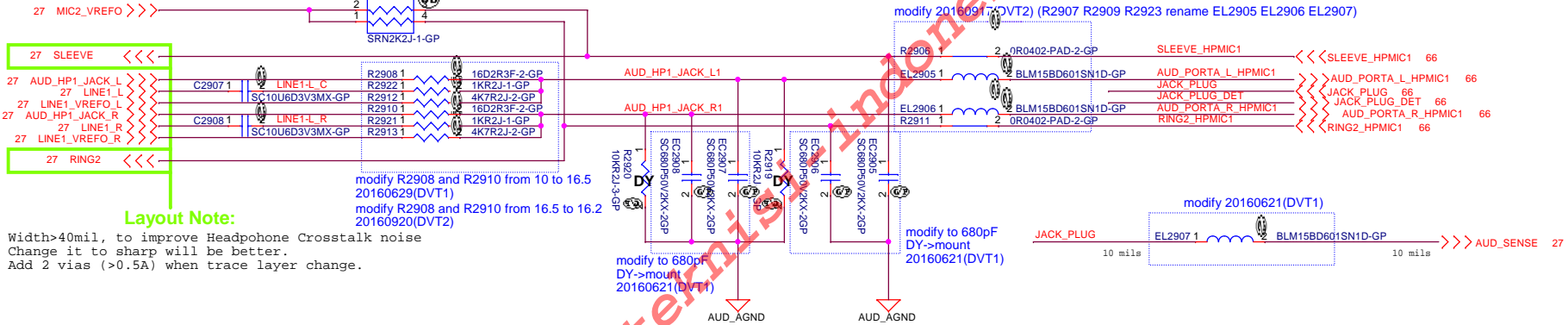
Speaker



CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R+
Pin4	SPK_R-

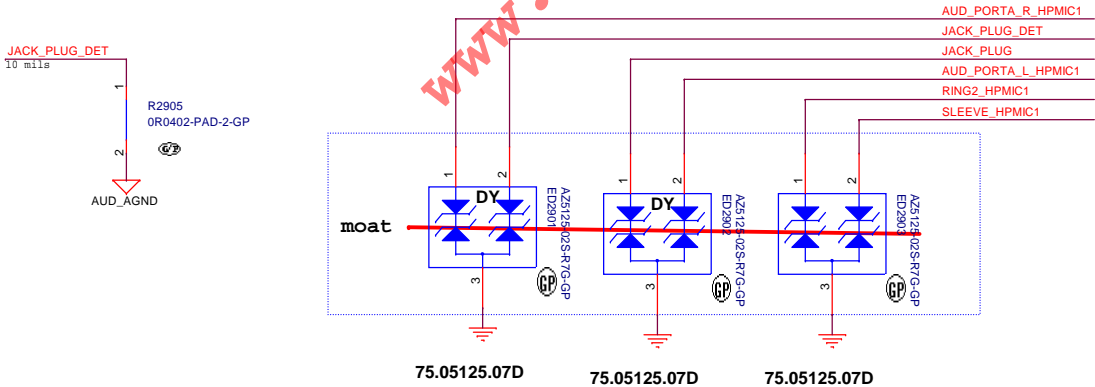
Universal Jack (Moved to I/O Board)

modify 20160621 (DVT1)



Layout Note:

Width>40mil, to improve Headphone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.




Main Func = Audio

(Blanking)

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<Core Design>



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Title

(Reserved)

Size
A4

Document Number
Keystone 13.3"

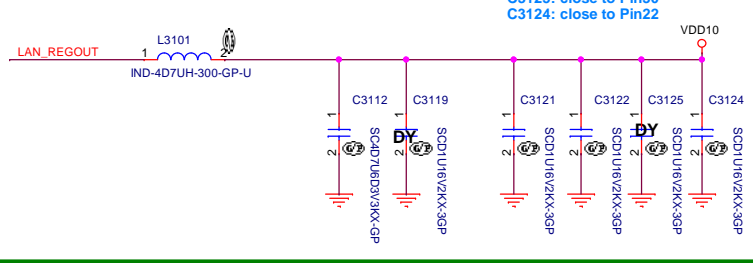
Rev
X00

Date: Wednesday, November 23, 2016

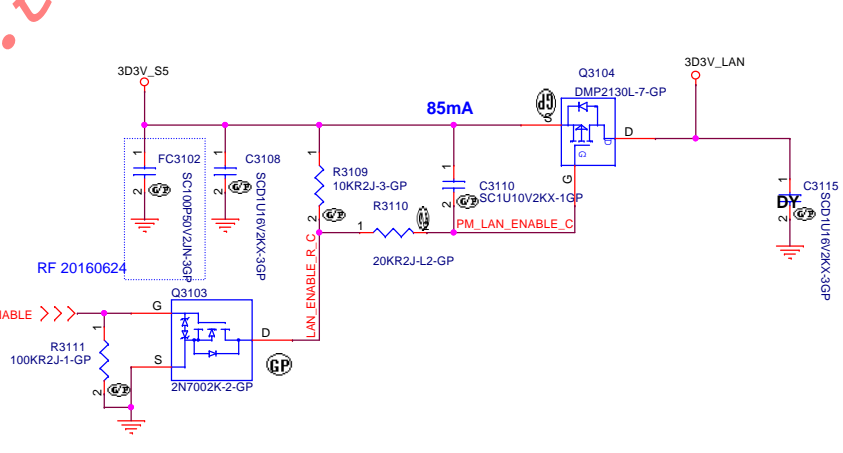
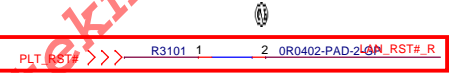
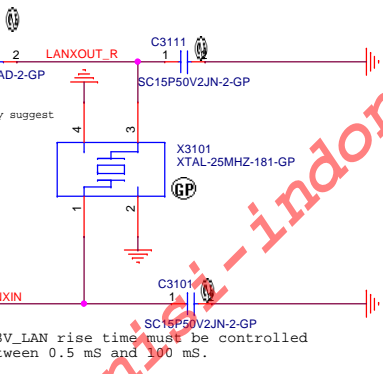
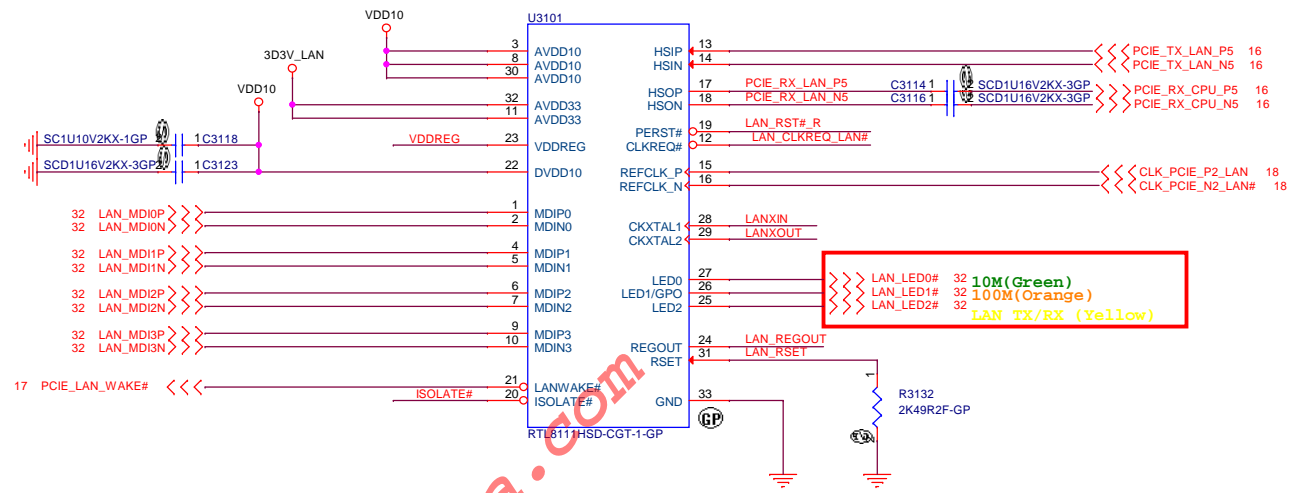
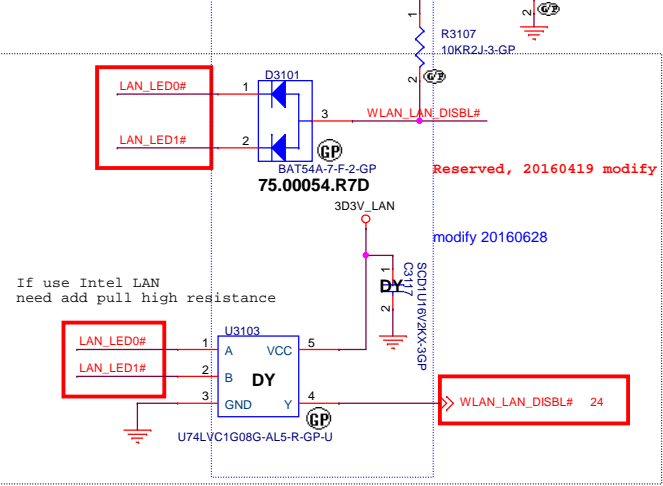
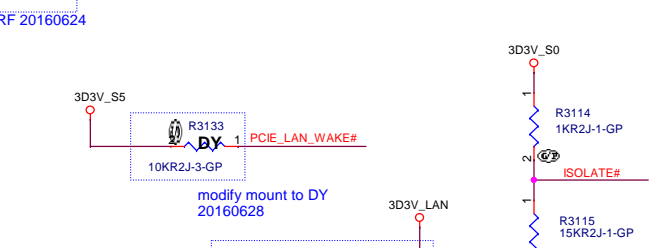
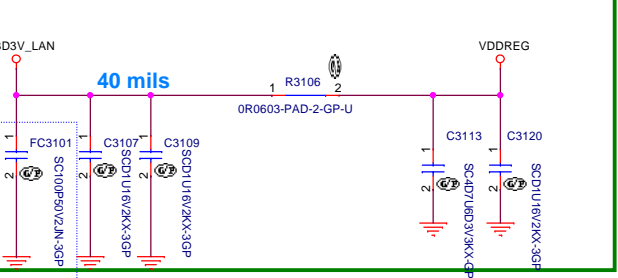
Sheet 30 of 106

SSID = LAN

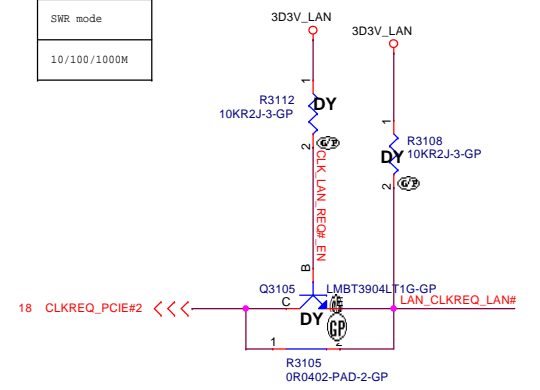
Layout:
* Place C3121 to C3124 close to each VDD10 pin--3, 8, 22, 30



Layout:
* Place C3107 and C3108 close to each VDD33 pin-- 11, 32



RTL8111HSD-COT
071.8111H.M001
SWR mode
10/100/1000M



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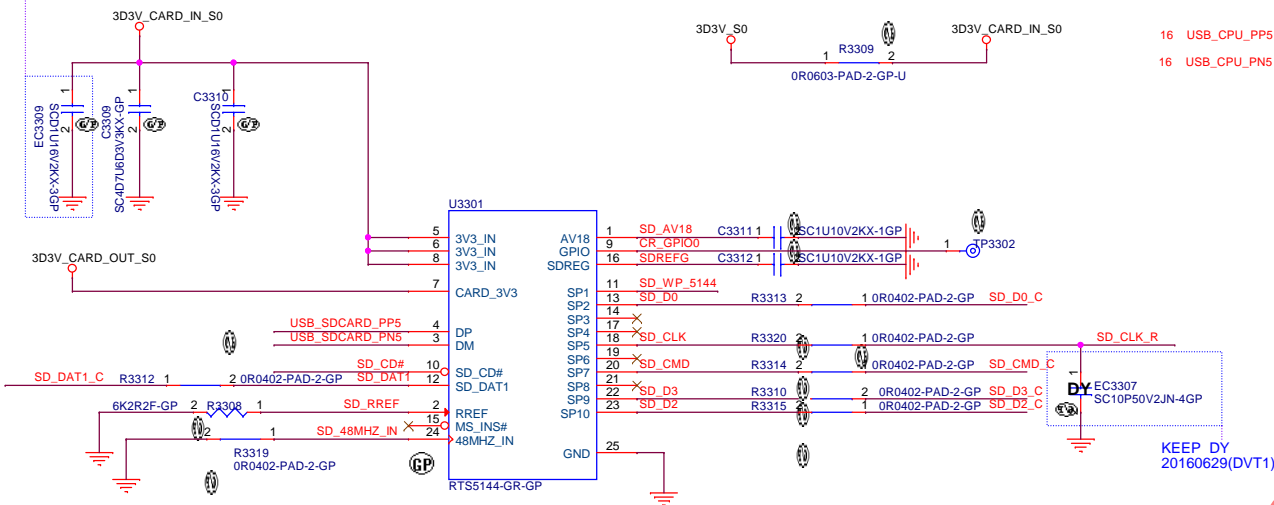
Title: **LAN**

Size: A3 Document Number: **Keystone 13.3"** Rev: **X00**

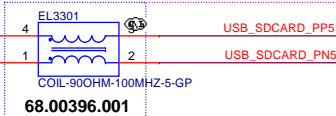
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Main Func = Card Reader

modify DY->mount
20160621(DVT1)

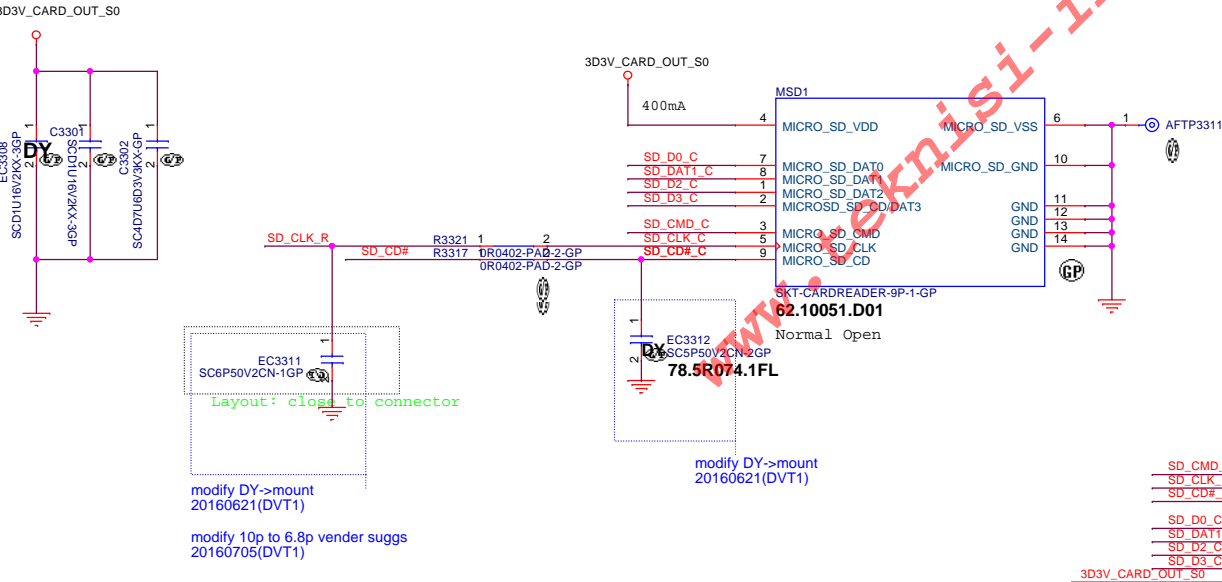
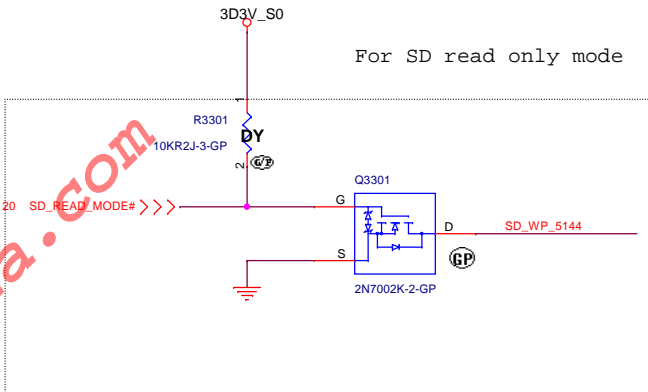


remove co-lay R3304 R3305
20161117(X1)

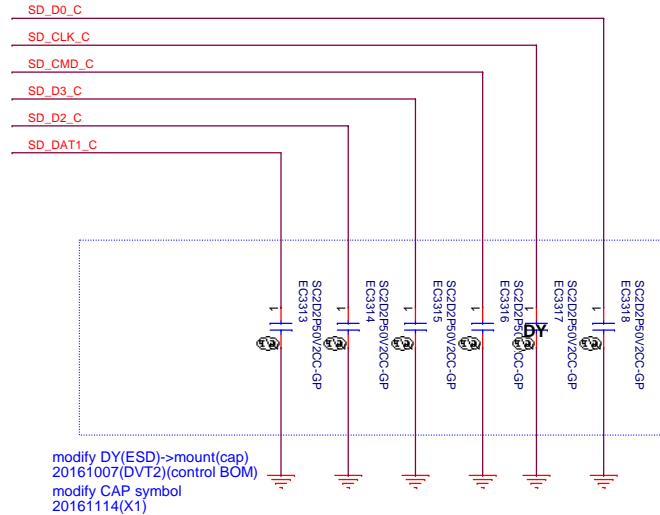


modify EL3301
part number
for common part
20160620

For SD read only mode



For EMI Reserved



<Core Design>



Title

Card Reader-RTS5144

Size

Document Number

Keystone 13.3"

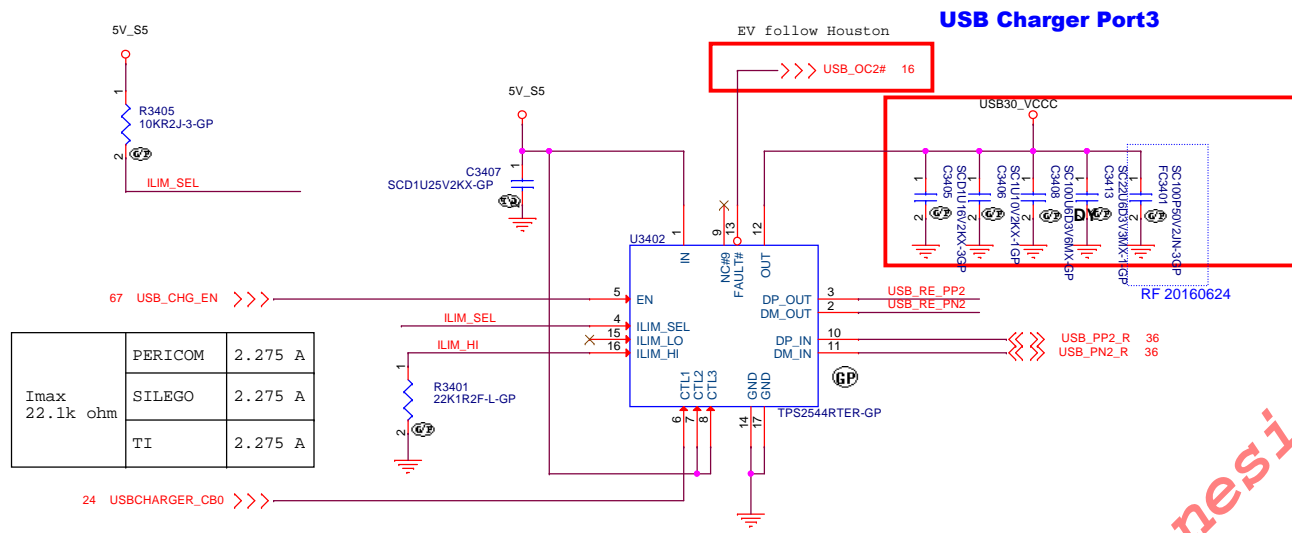
Date:

Wednesday, November 23, 2016

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ev

Main Func = USB3.0 Port1

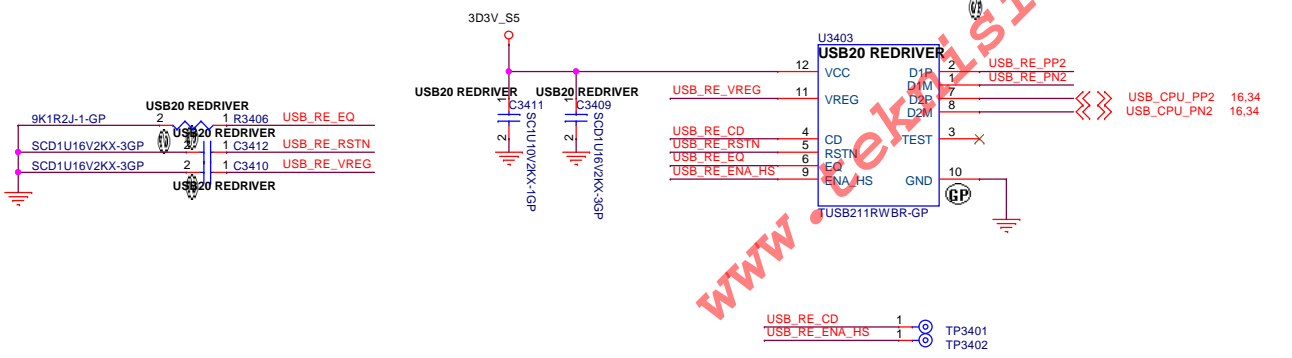


PI5USB2544 Device Control Pins Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	
0	x	1	x	DCP_Auto	ILIM_HI	Data lines disconnected
0	1	0	0	SDP1	ILIM_LO	Data lines connected
0	1	0	1	SDP1	ILIM_HI	Data lines disconnected
0	1	1	0	DCP_Auto	ILIM_HI	Data lines disconnected
0	1	1	1	DCP_Auto	ILIM_HI	Data lines disconnected
1	0	0	0	DCP_Shorted	ILIM_LO	Device forced to stay in DCP BC1.2 charging mode
1	0	1	0	Divider-1A	ILIM_LO	Device forced to stay in Divider-1A charging mode
1	0	1	1	Divider-1A	ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	
1	1	0	1	SDP1	ILIM_HI	Data lines connected
1	1	1	0	SDP2 ⁽¹⁾	ILIM_LO	
1	1	1	1	CDP ⁽¹⁾	ILIM_HI	Data lines connected

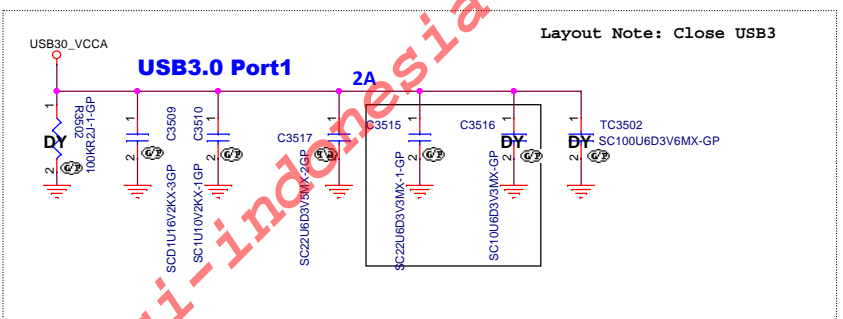
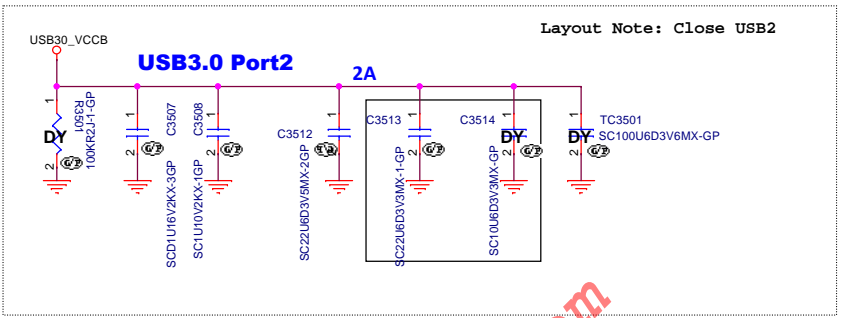
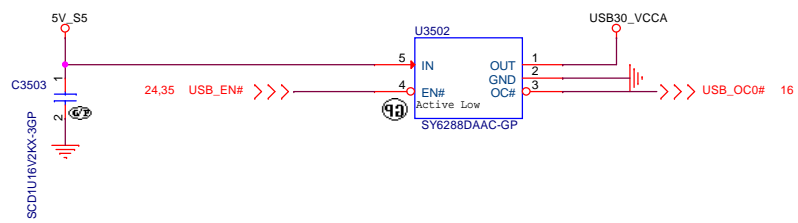
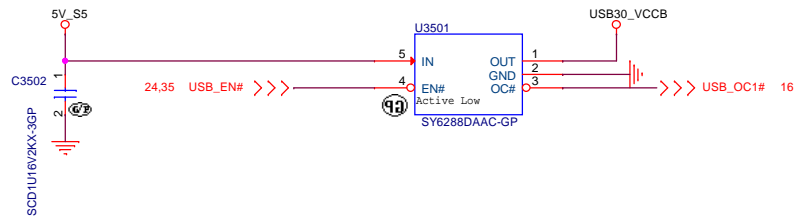
Note:
(1) No OUT discharge when changing between 1111 and 1110.

USB2.0 Redriver



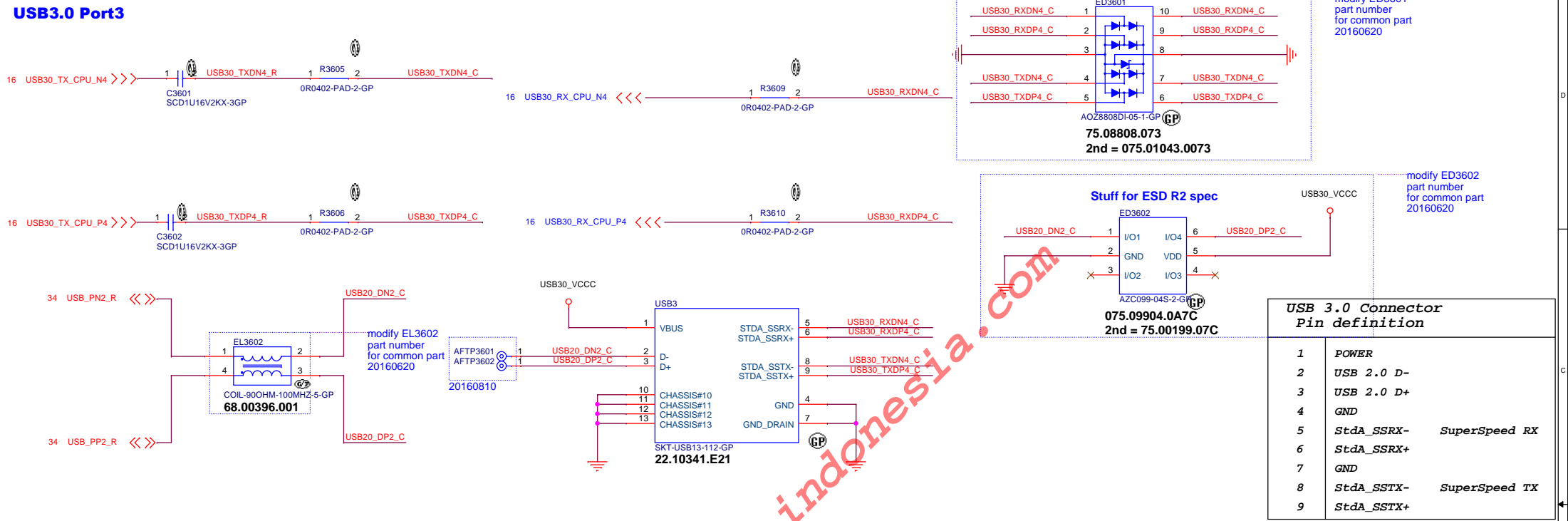
EQ gain setting	R1 [ohms]
Level 0	100 +/- 5%
Level 1	1800 +/- 5%
Level 2	3900 +/- 1%
Level 3 [MIN]	9100 +/- 5%

Main Func = USB3.0 Port1



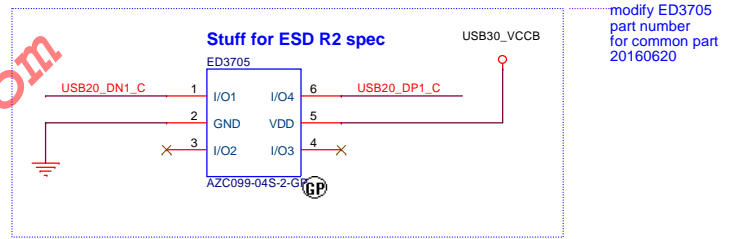
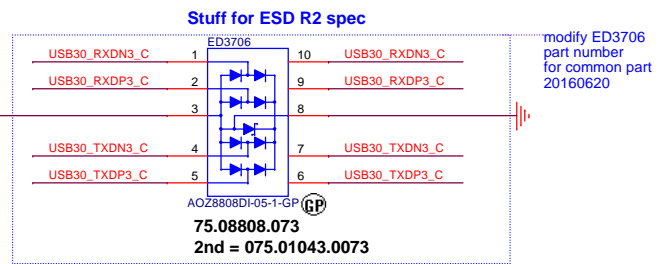
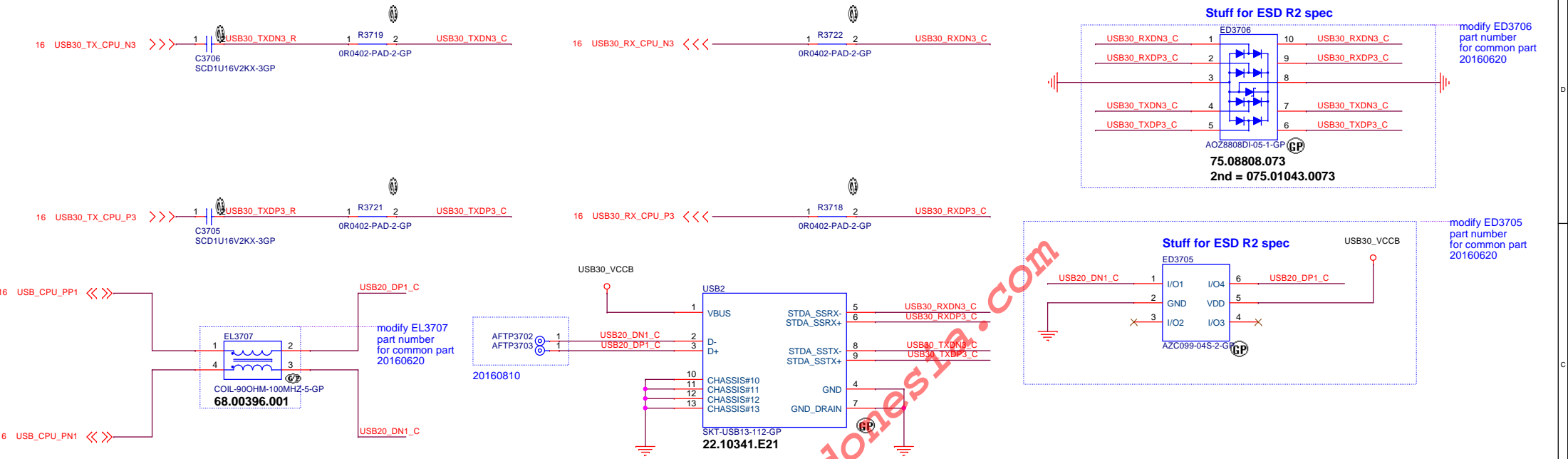
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Main Func = USB3.0 Port1

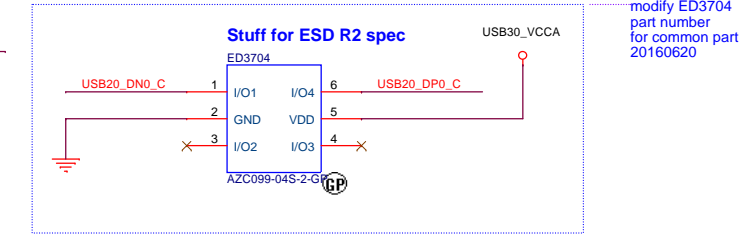
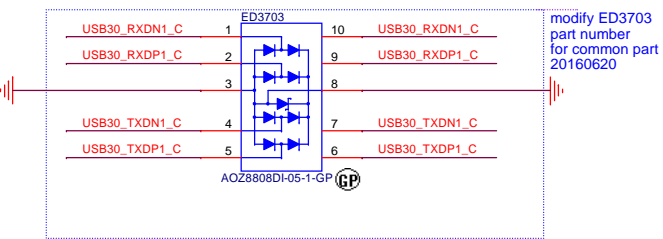
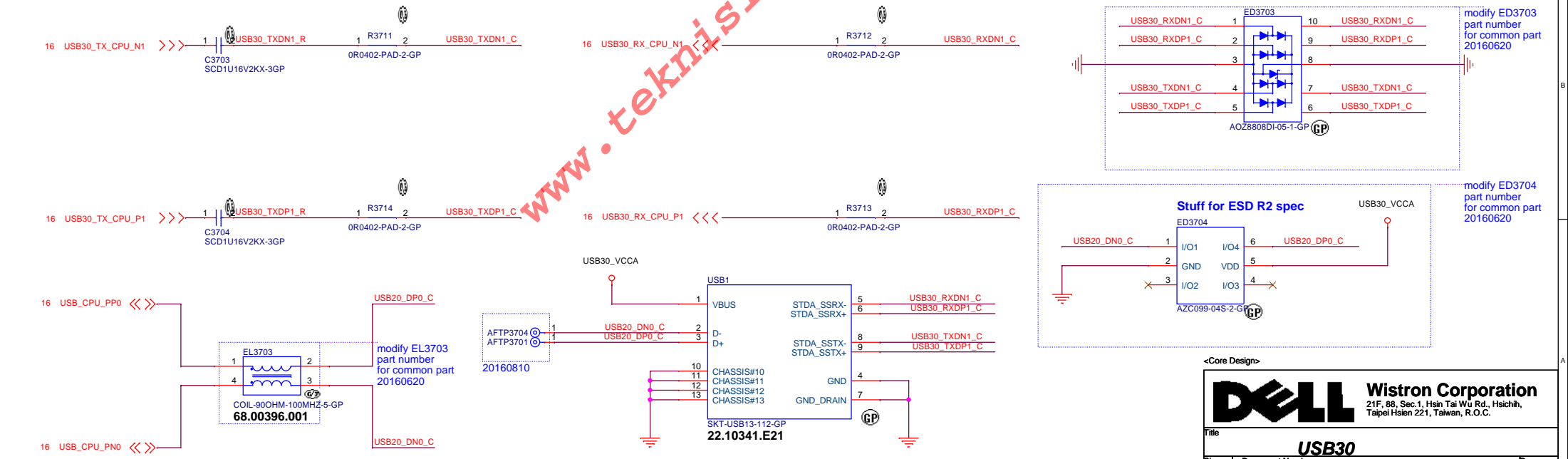


Main Func = USB3.0 Port1

USB3.0 Port2



USB3.0 Port1



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Title: **USB30**

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Main Func = USB3.0 Port1

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new project,
help to use cost down version
88C10CAC for instead.

U4101_OUT

3D3V_S5_PCH

U4101

DS3

R4103

0R0603-PAD-2-GP-U

C4101

DS3

SY6288C10CAC-GP

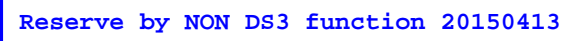
GP

(OBS)

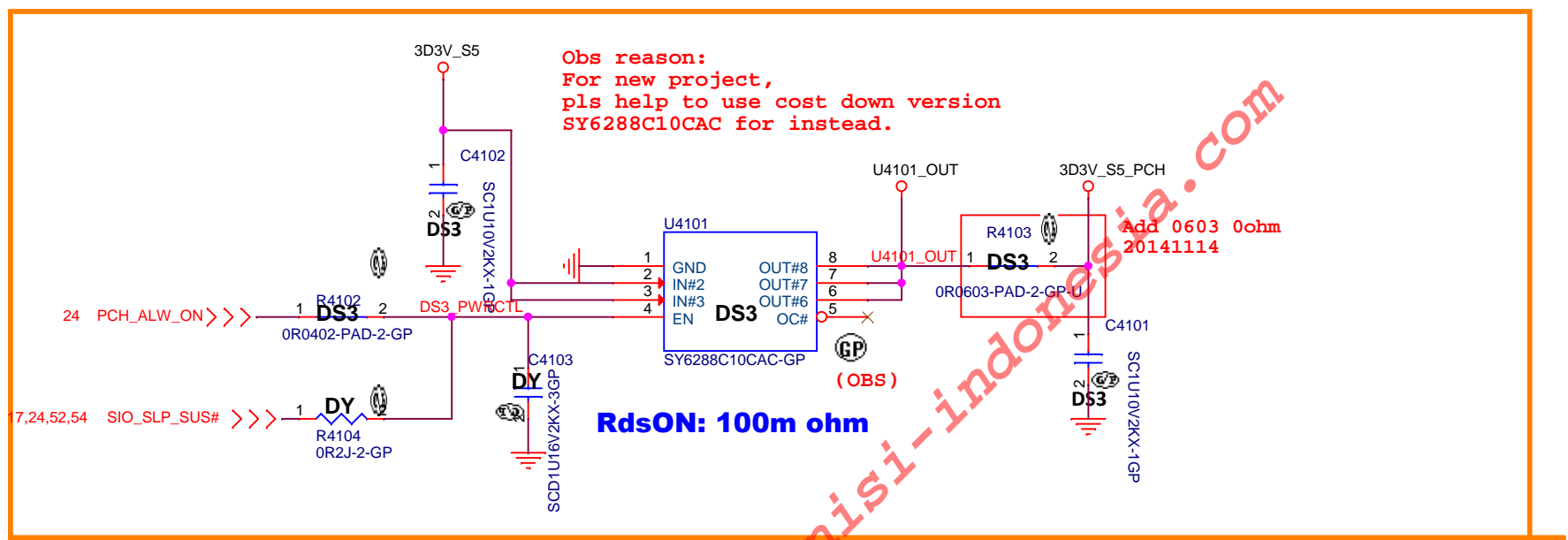
dsON: 100m ohm

Add 0603 0ohm
20141114

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Obs reason:
For new project,
pls help to use cost down version
SY6288C10CAC for instead.




DS3

Main Func = DIMM1
Main Func = DIMM2

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<Core Design>



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Title

Connected_Standby(2/2)

Size

Document Number

Rev

A3

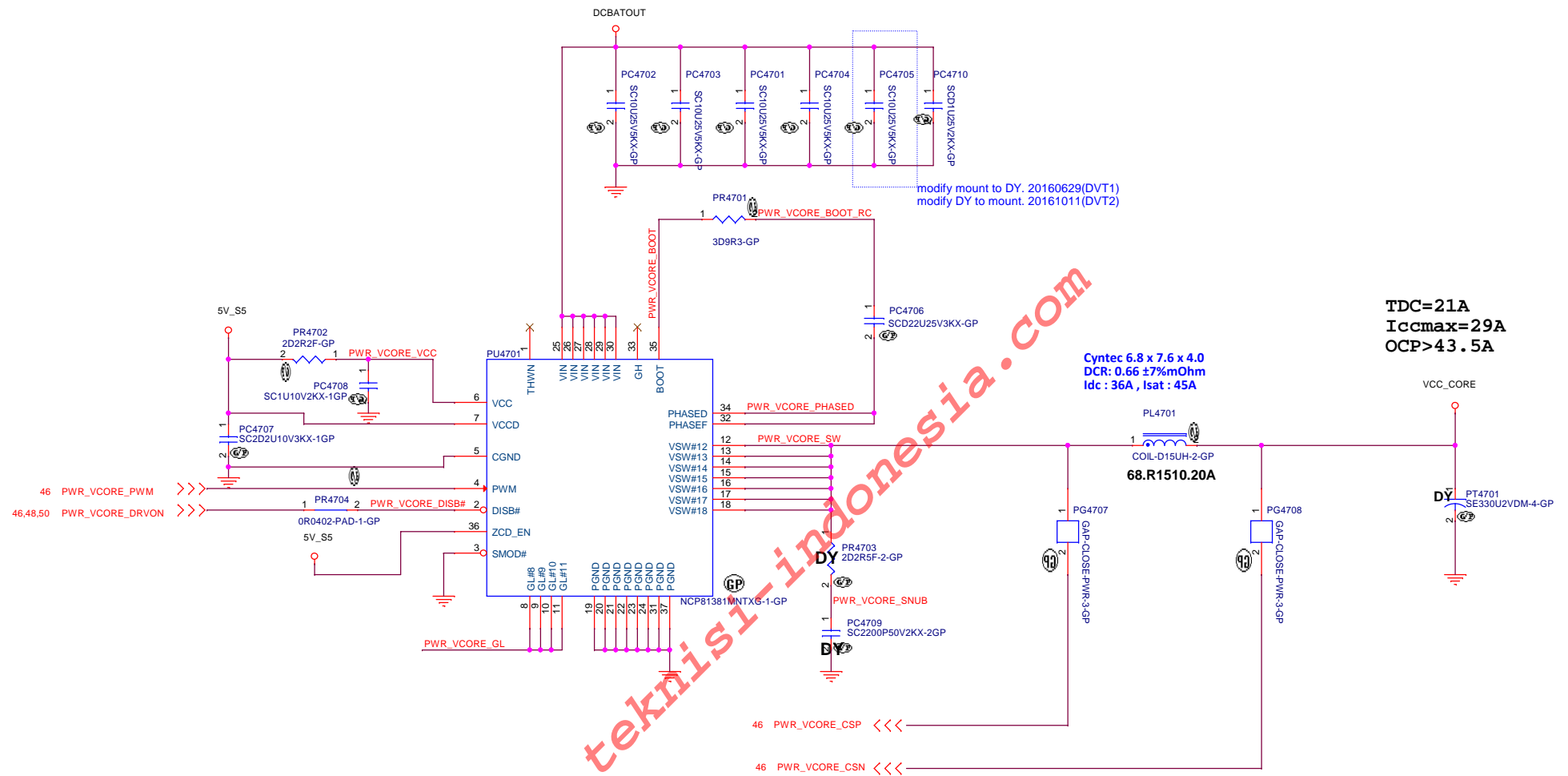
Keystone 13.3"

X00

Date: Wednesday, November 23, 2016

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```
Main Func = CPU_CORE
```



<Core Design>



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Title	Author	Year	Journal	Volume	Page
...

NCP81382MN_CPU_VCORE(2/3)

Size
A3

Document Number

Keystone 13.3"

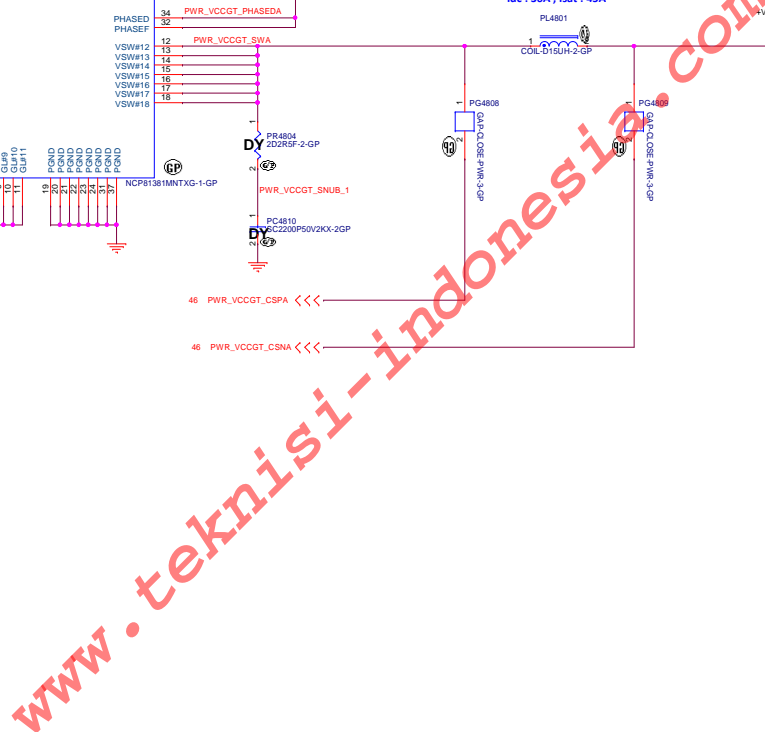
ev

X00

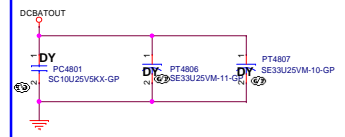
Date: Wednesday, November 23, 2016

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Main Func = VCCGT



PCBATOUT



TDC=18A
Iccmax=31A
OCP>46.5A

Cyntec 6.8 x 7.6 x 4.0
DCR: 0.66 ± 7% mOhm
Idc : 36A , Isat : 45A

«Core Design»



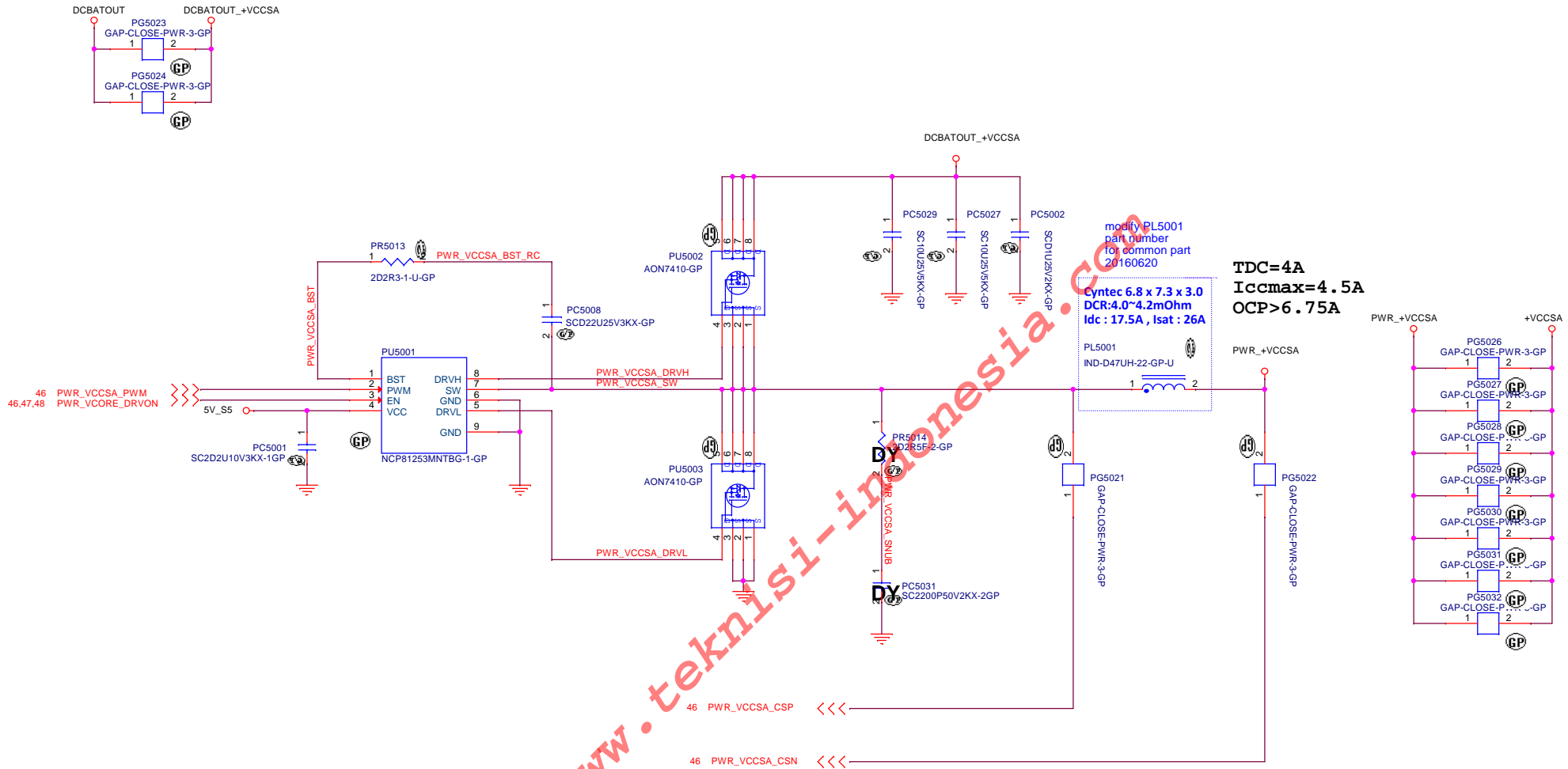
Title **NCP81382MN_CPU_VCCGT(3/3)**

Size A2	Document Number Keystone 13.3"	Rev X0
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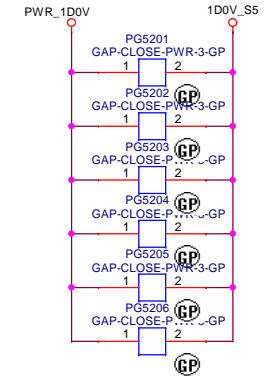
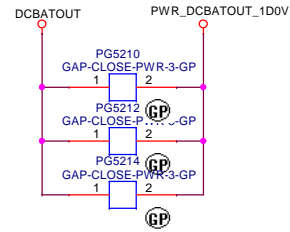
Date: Wednesday, November 23, 2016 Sheet 48 of 106

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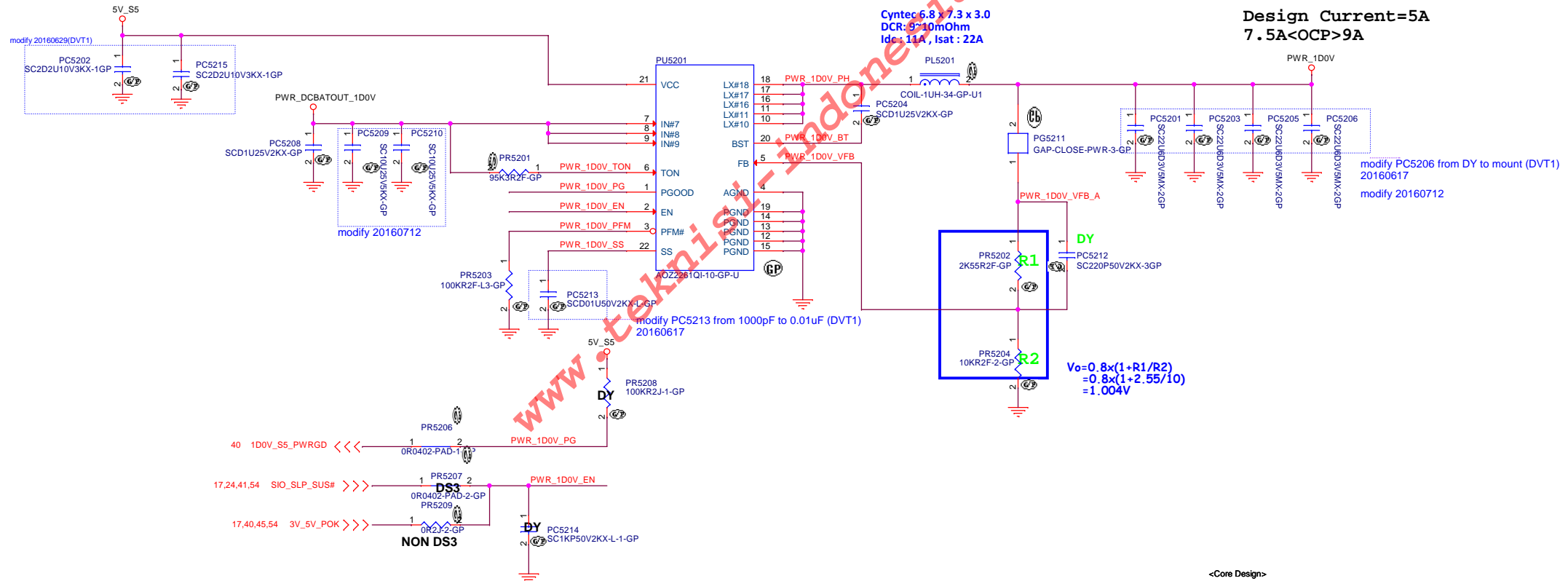
Main Func = CPU_CORE




```
SSID = PWR.Plane.Regulator_1D0V
```



AOZ2261 for 1D0V



<Core Design>



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Title

(Reserved)

Size
A3

Document Number	
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X00


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106

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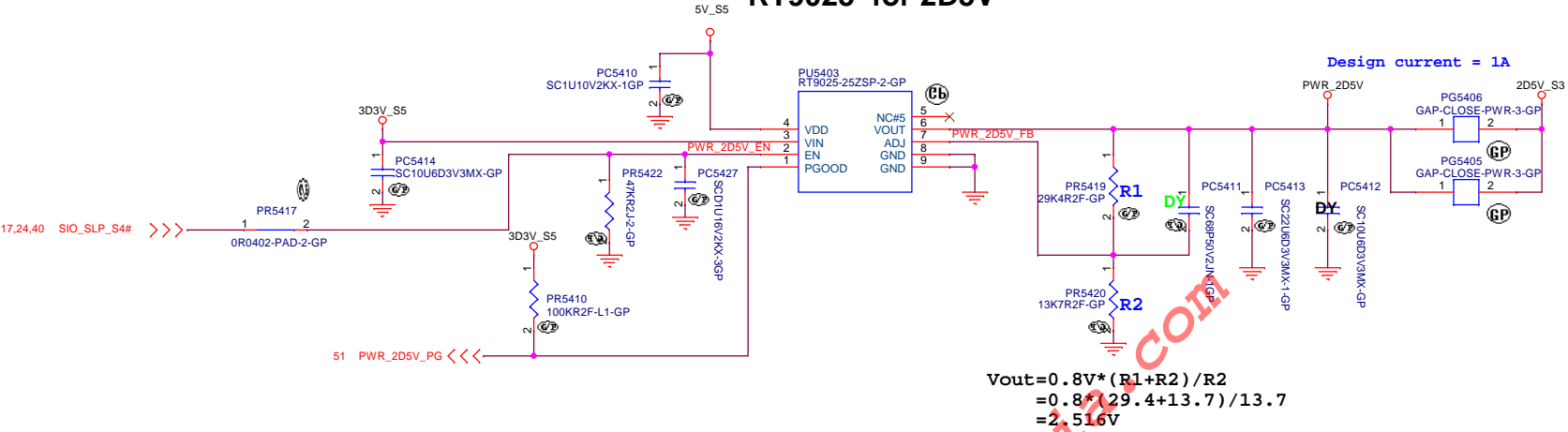
Title

(Reserved)

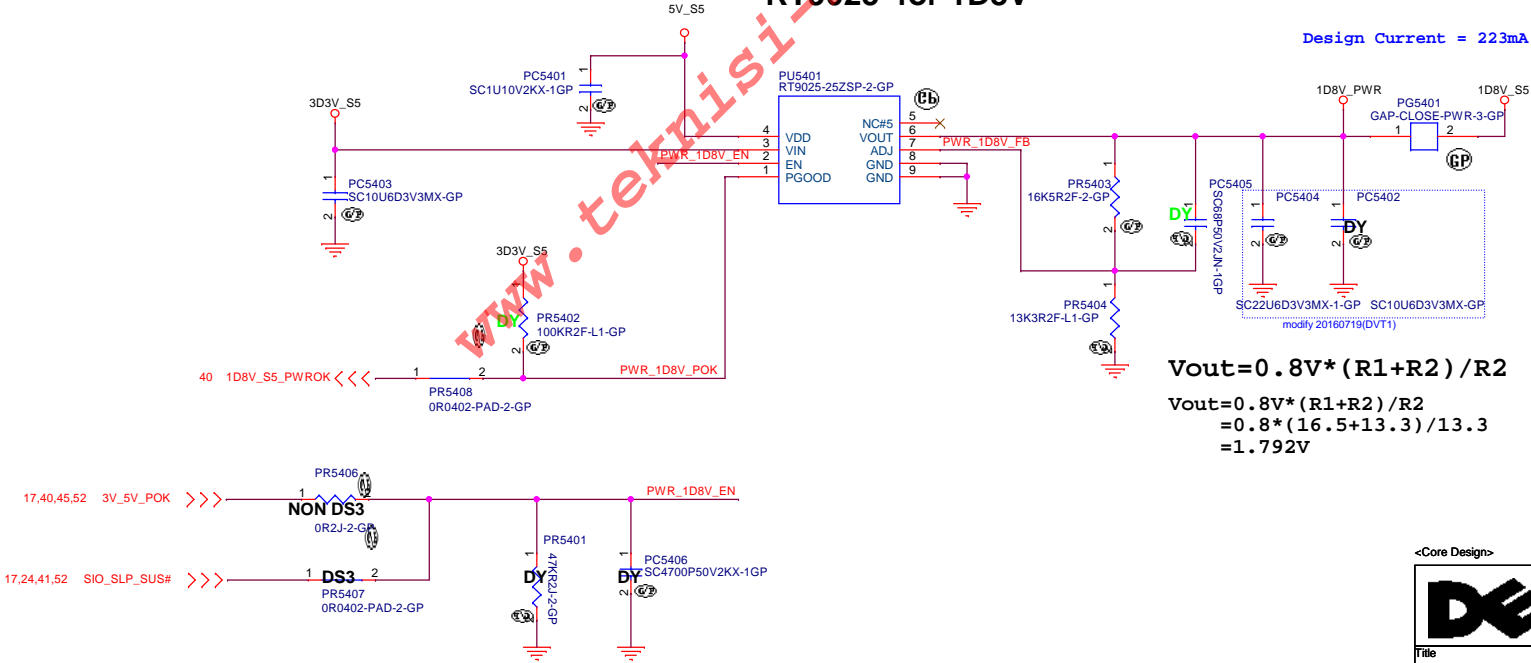
Size	Document Number	Rev
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RT9025 for 2D5V

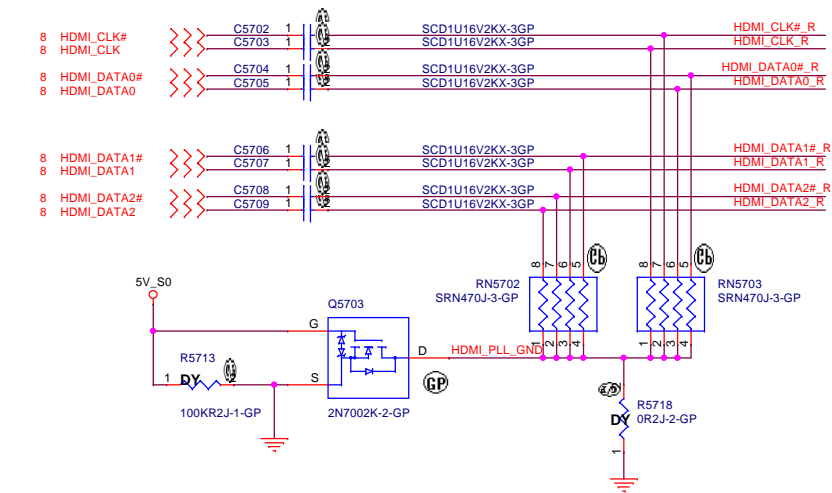


RT9025 for 1D8V



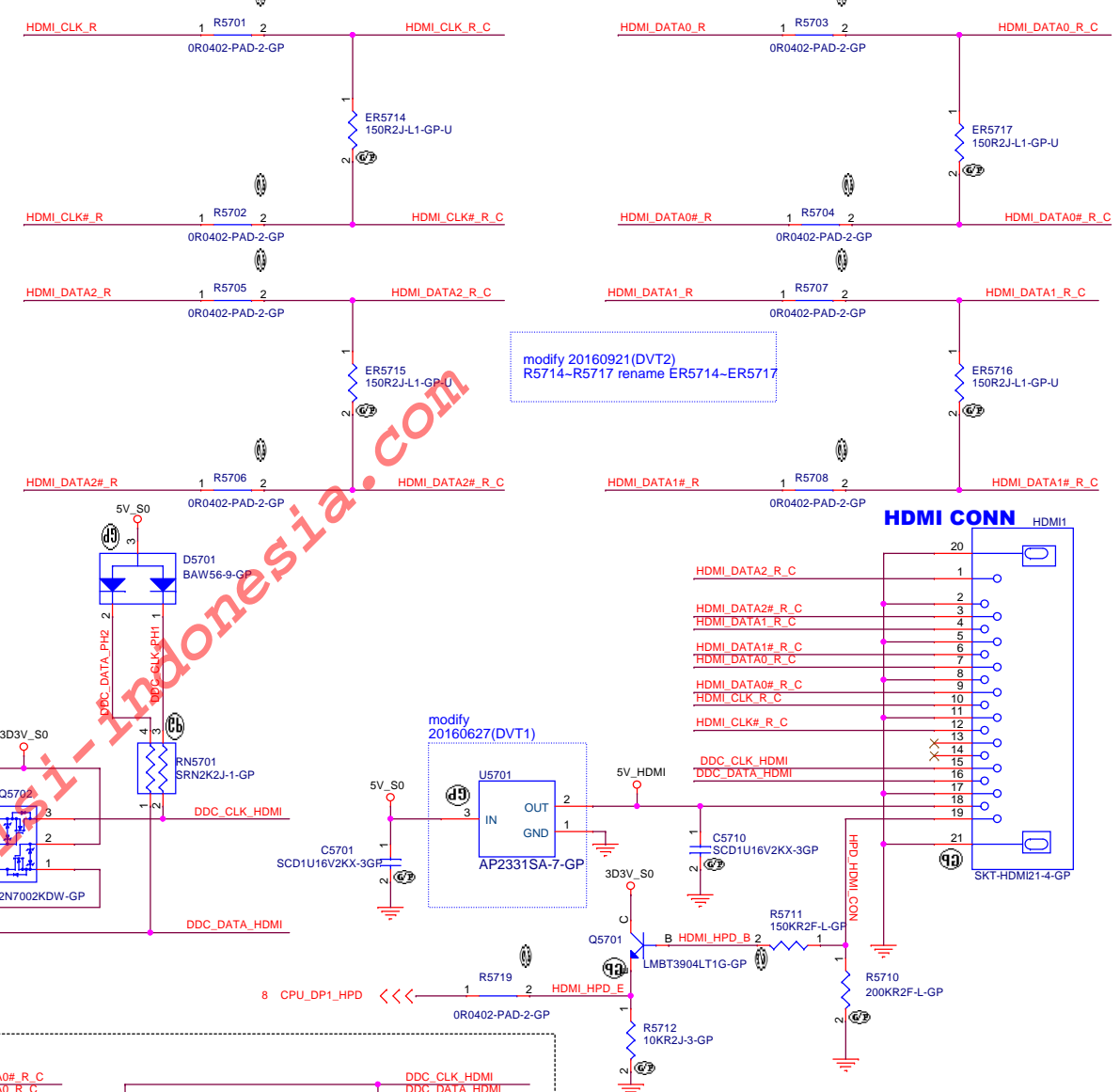
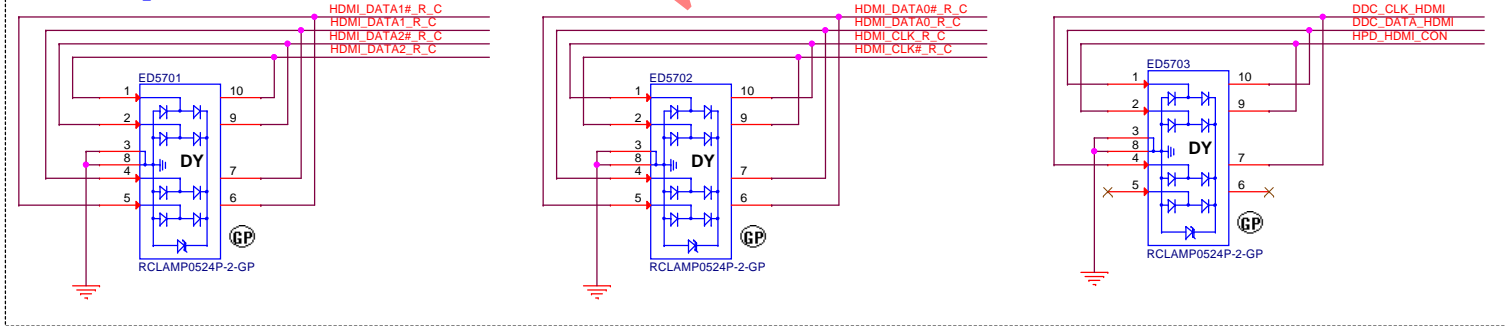
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Main Func = HDMI



remove R5709, F5701 (5V_HDMI_S0)
20160627(DVT1)

EMI Request:



<Core Design>

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Title	HDMI	
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Title			(Reserved)		
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(Blanking)

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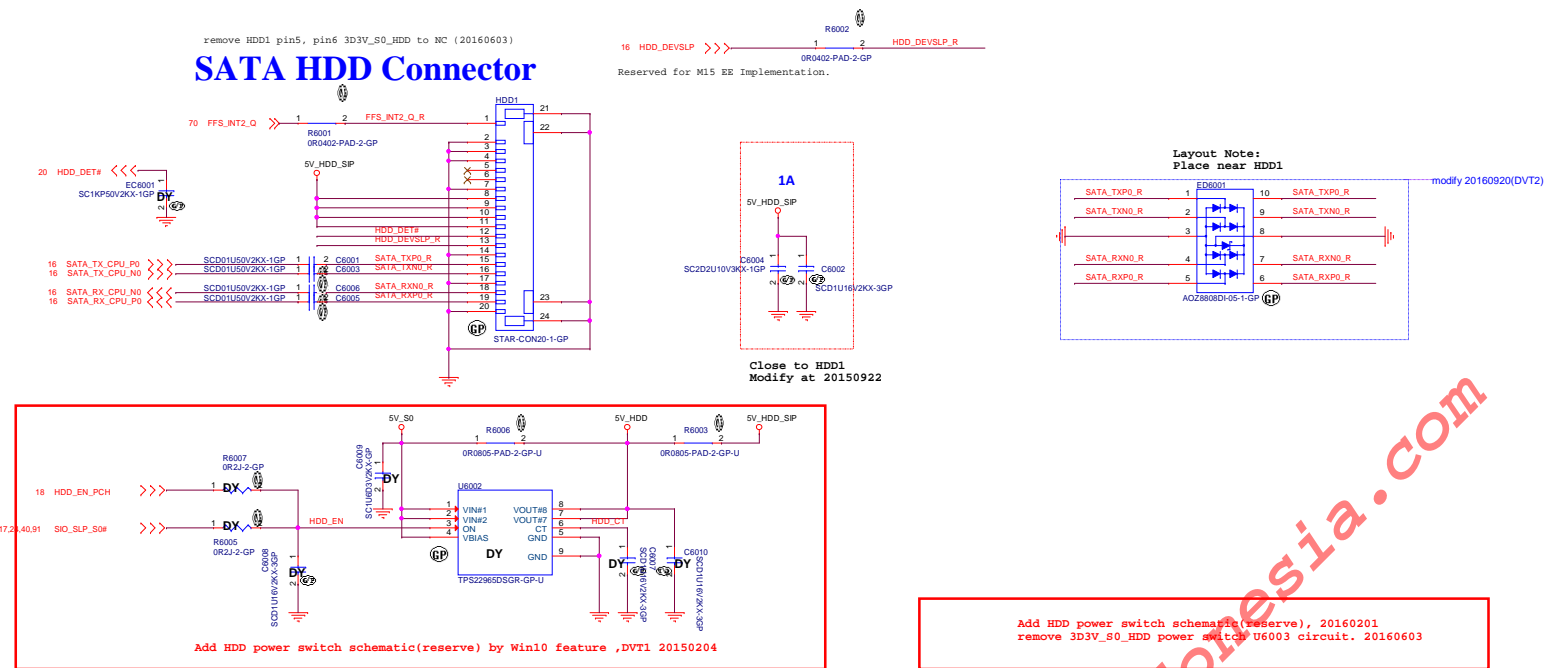
<Core Design>



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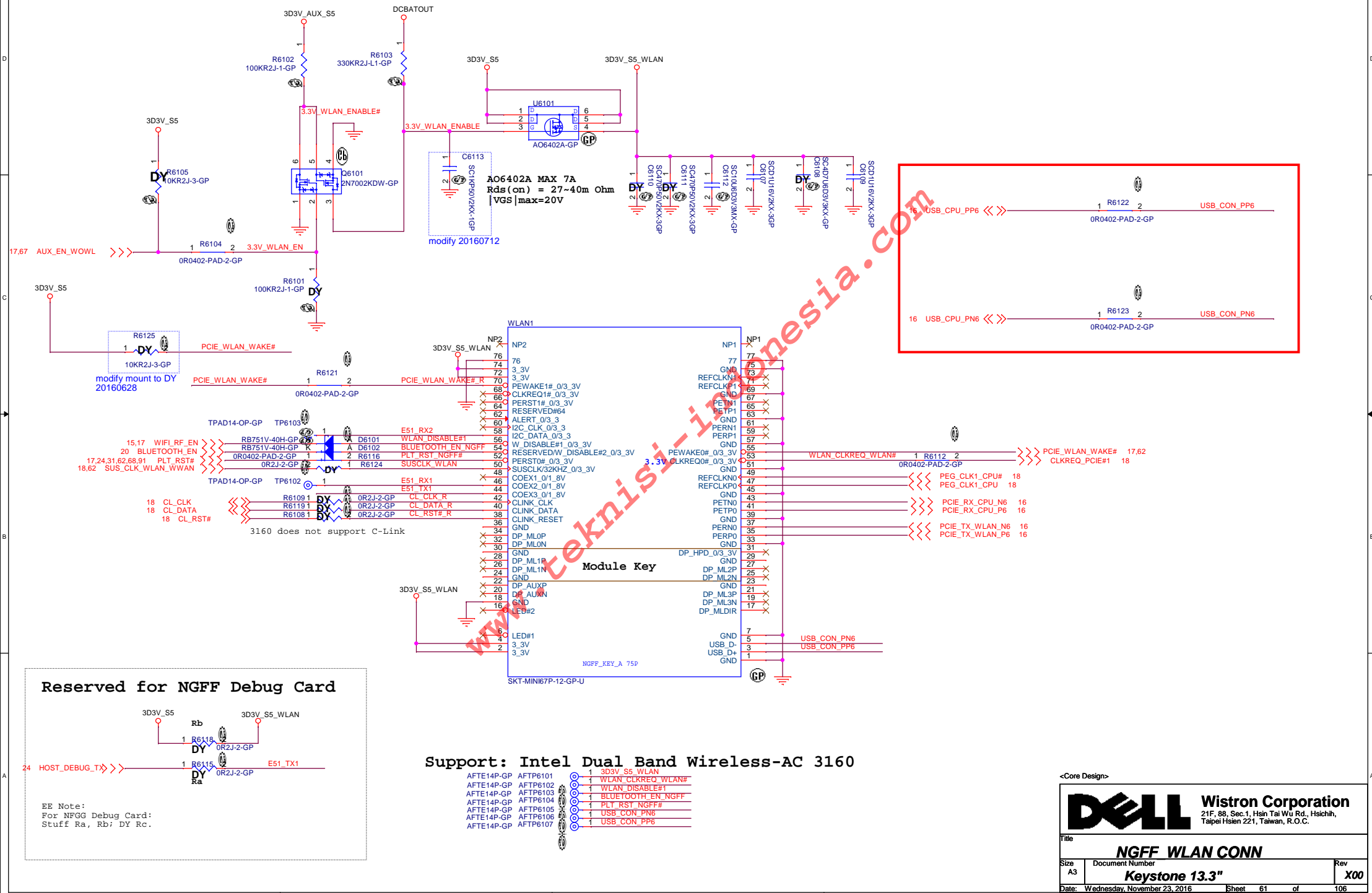
Title			(Reserved)		
Size	Document Number				Rev
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Main Func = HDD

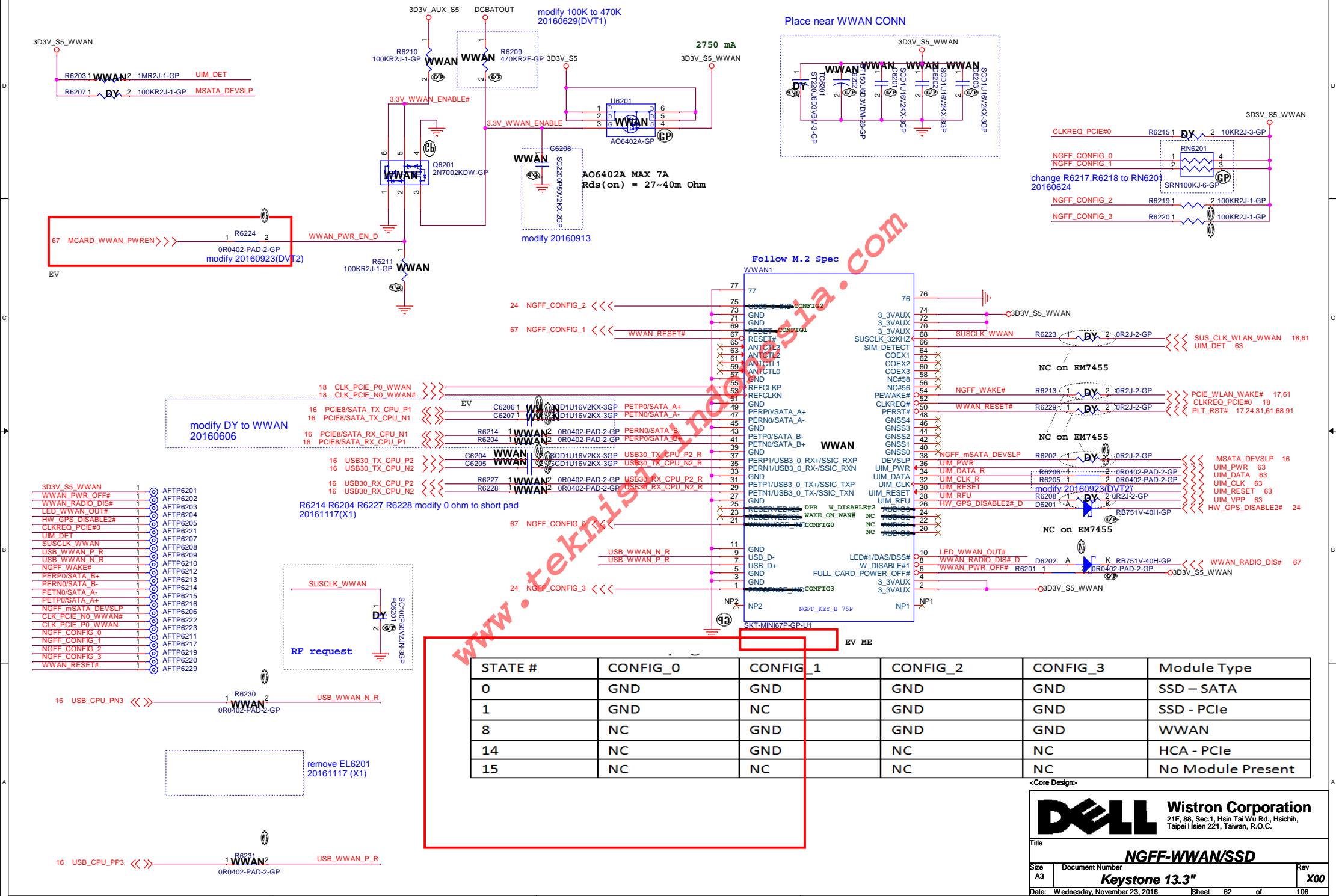


Main Func = ODD

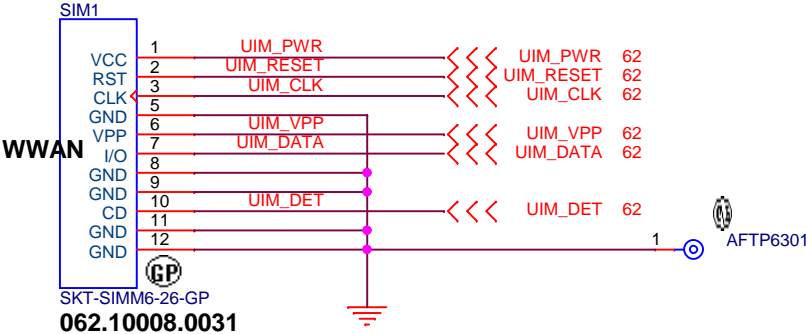
Main Func = WLAN



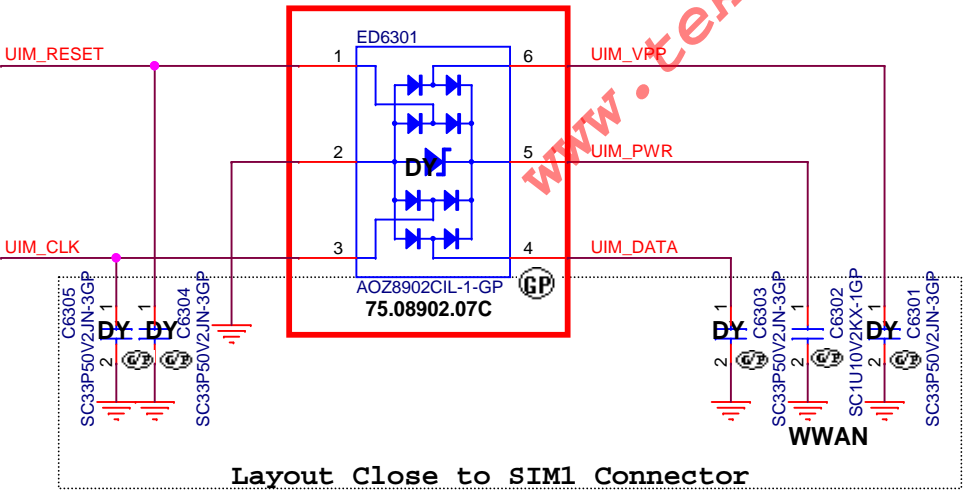
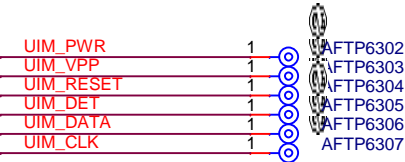
NGFF(WWAN/SSD)




SSID =WIRELESS



PIN	062.10008.0031 Micro SIM PinDefine
1	VCC
2	RST
3	CLK
5	GND
6	VPP
7	I/O
8	GND
9	GND
10	SIM Card Detect
11	GND
12	GND



<Core Design>



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Title

uSIM

Size

Document Number

Rev

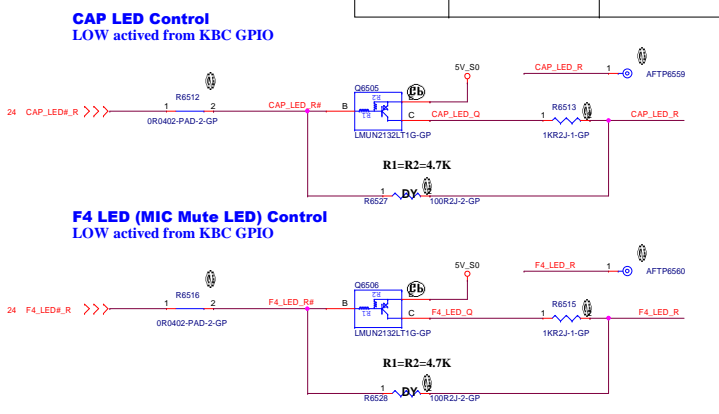
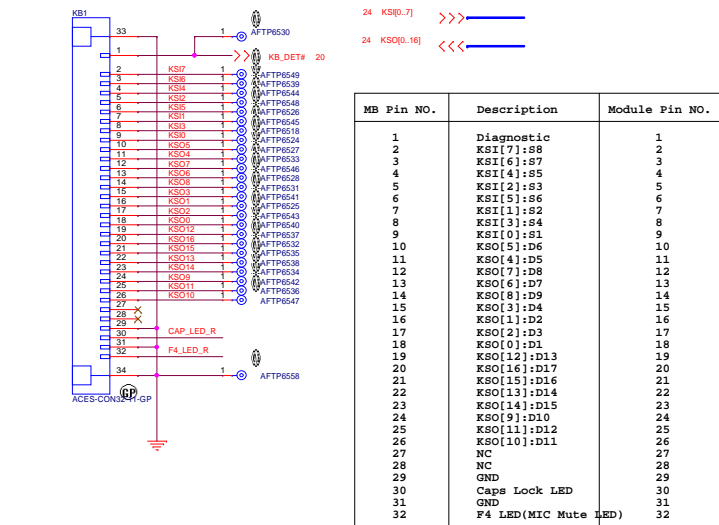
Keystone 13.3"

X00

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Internal KeyBoard Connector



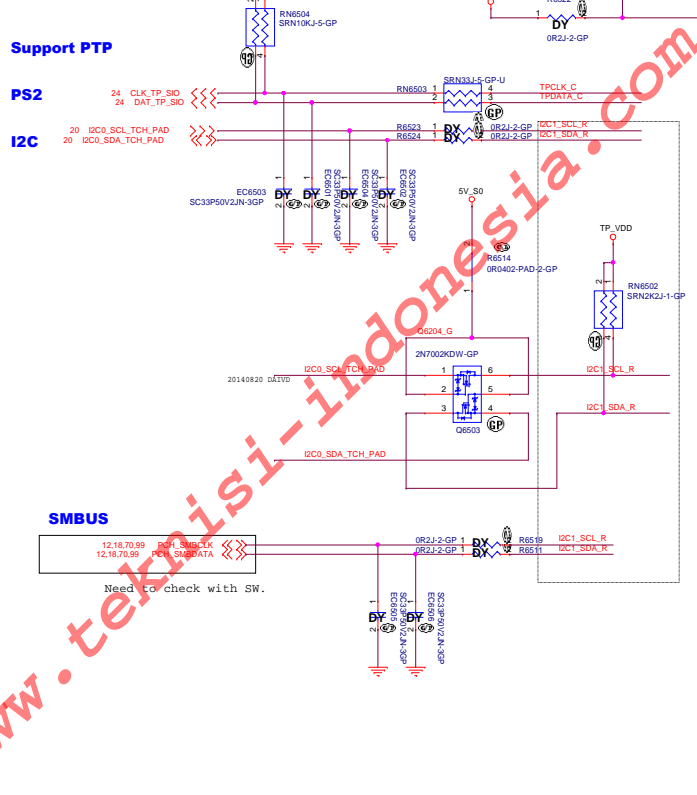
Support PTP

PS2

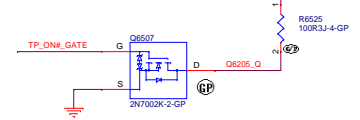
I2C

SMBUS

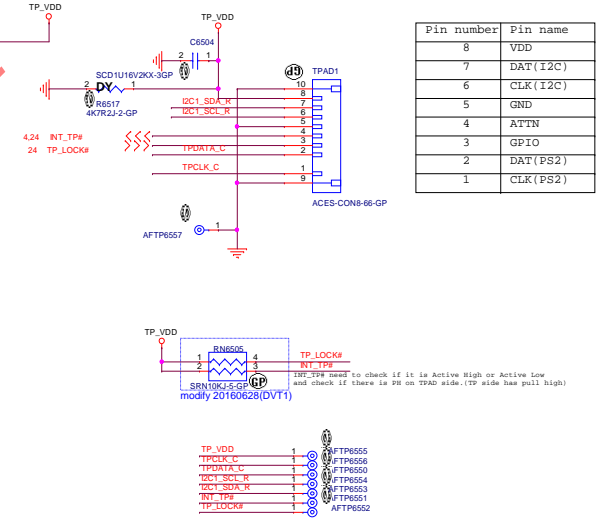
Need to check with SW.



TP_VDD Discharge Circuit

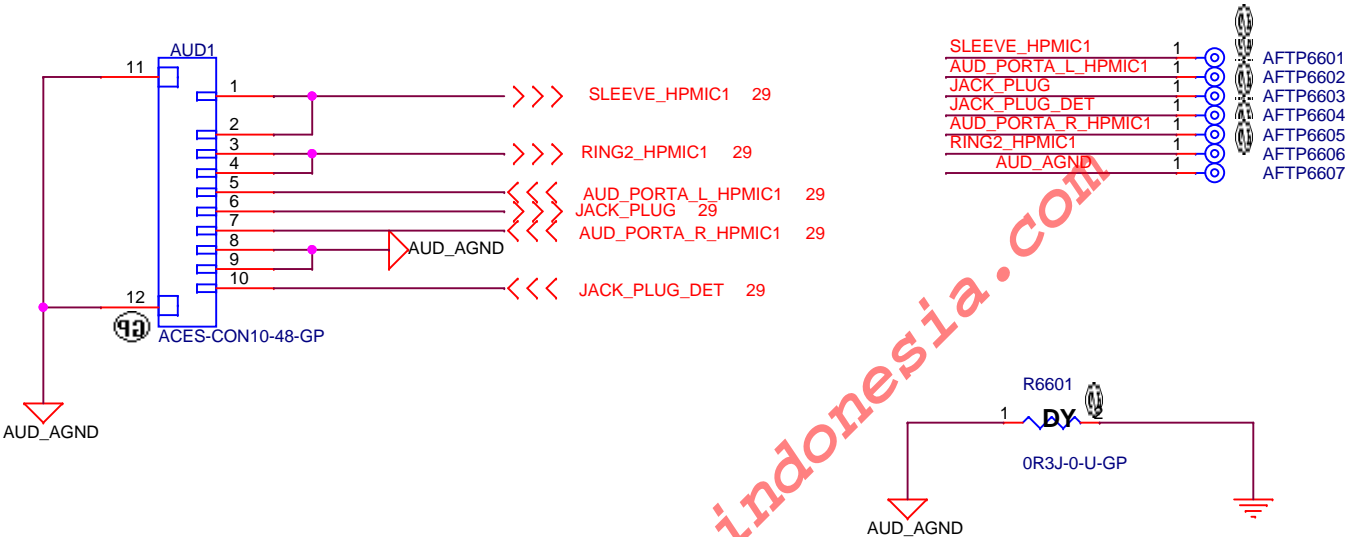


Precision Touch Pad Connector



Main Func = IO Connector

I/O Board Connector



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Title

IO Board Connector

Size
A4

Document Number
Keystone 13.3"

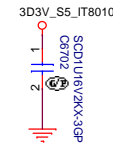
Rev
X00

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GPIO Expander

PLACE CLOSED TO PIN



All I/O Signals are 3.3V CMOS Level

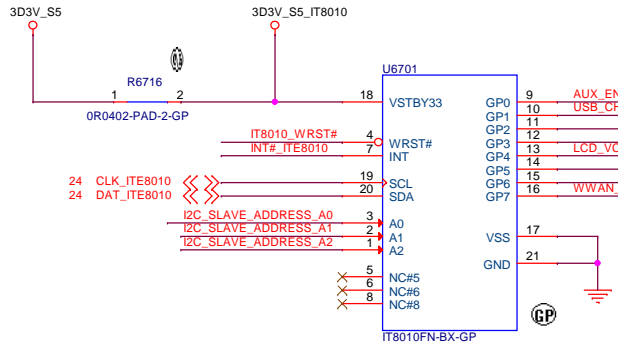
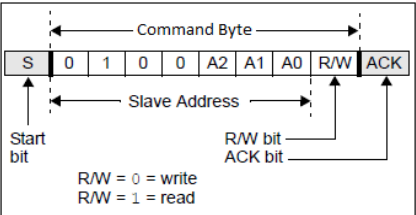
IT8010/IT8011/IT8012 difference

DEVICE	PIN8	PIN18
IT8010	NC	VSTBY33
IT8011	NC	VSTBY18
IT8012	VCOREI	VSTBY33

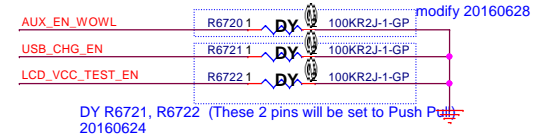
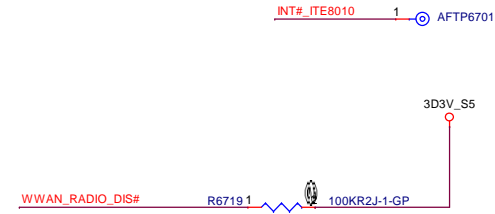
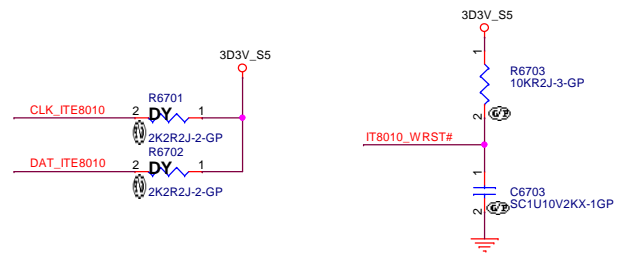
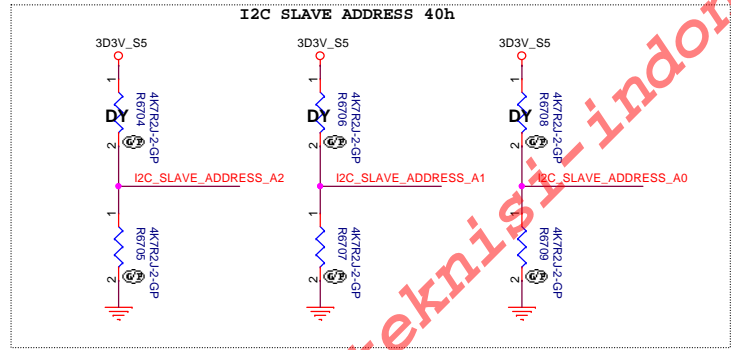
I2C SAD*Read/Write patterns

Command SAD[7:4], A[2], A[1], A[0], R/W= SAD*R/W

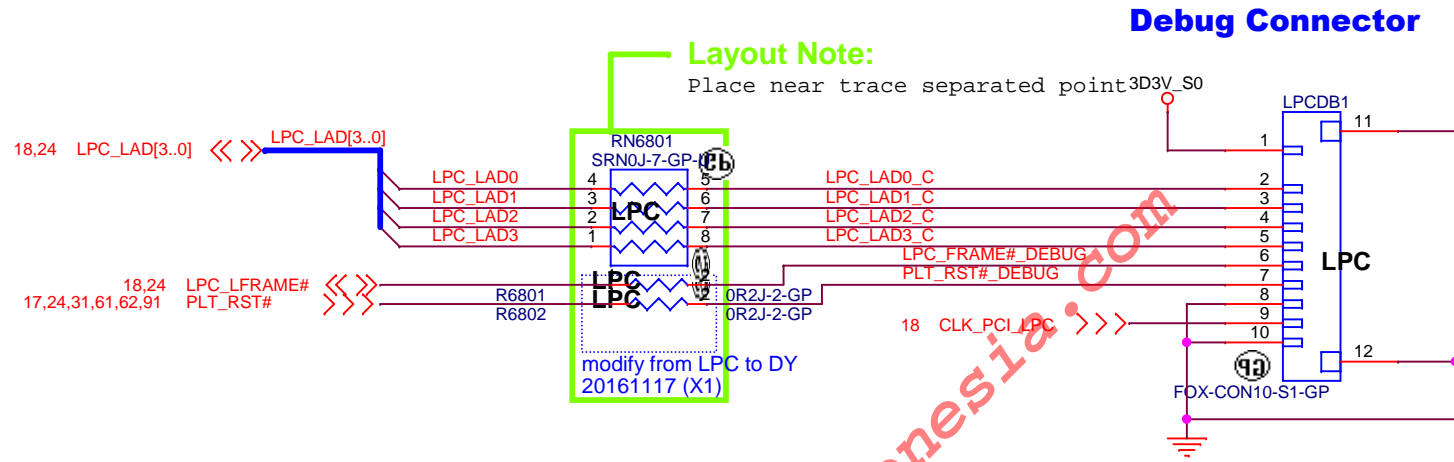
Read	0100	0	0	0	0	1	01000001 (41b)
Write	0100	0	0	0	0	0	01000000 (40h)
Read	0100	0	0	1	1	0	01000011 (43h)
Write	0100	0	0	1	0	0	01000010 (42h)
Read	0100	1	1	1	1	0	01001111 (4Fh)
Write	0100	1	1	1	0	0	01001110 (4Eh)



(U6701 DVT2 use 071.23008.0003. BOM control)



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20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

<Core Design>

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Title Dubug connector			
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Title			Reserved	
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Title			RESERVED	
Size	Document Number	Rev		
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Title

USB3.0 PORT

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www.teknisi-indonesia.com

Main Func = dGPU

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Title

GPU(55)PWR/GND

Size

Document Number

Rev

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Main Func = dGPU

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<Core Design>



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Title

GPU-VRAM1,2 (1/4)

Size
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Rev
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Main Func = dGPU

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<Core Design>



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Title

GPU-VRAM3,4 (2/4)

Size

A3

Document Number

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Main Func = dGPU

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<Core Design>



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Title

GPU-VRAM5,6 (3/4)

Size
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Main Func = dGPU

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<Core Design>



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Title

GPU-VRAM7,8 (4/4)

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Main Func = dGFX_CORE

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Main Func = dGPU

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&ltCore Design>



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Title _____

GPU Discrete Power	
1	100
2	100
3	100
4	100
5	100
6	100
7	100
8	100
9	100
10	100
11	100
12	100
13	100
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Title

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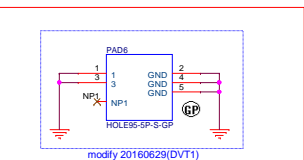
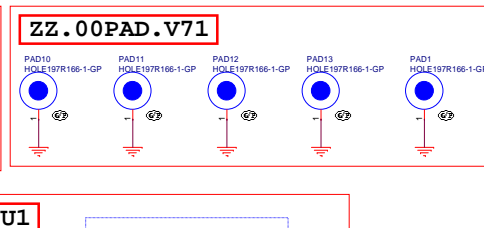
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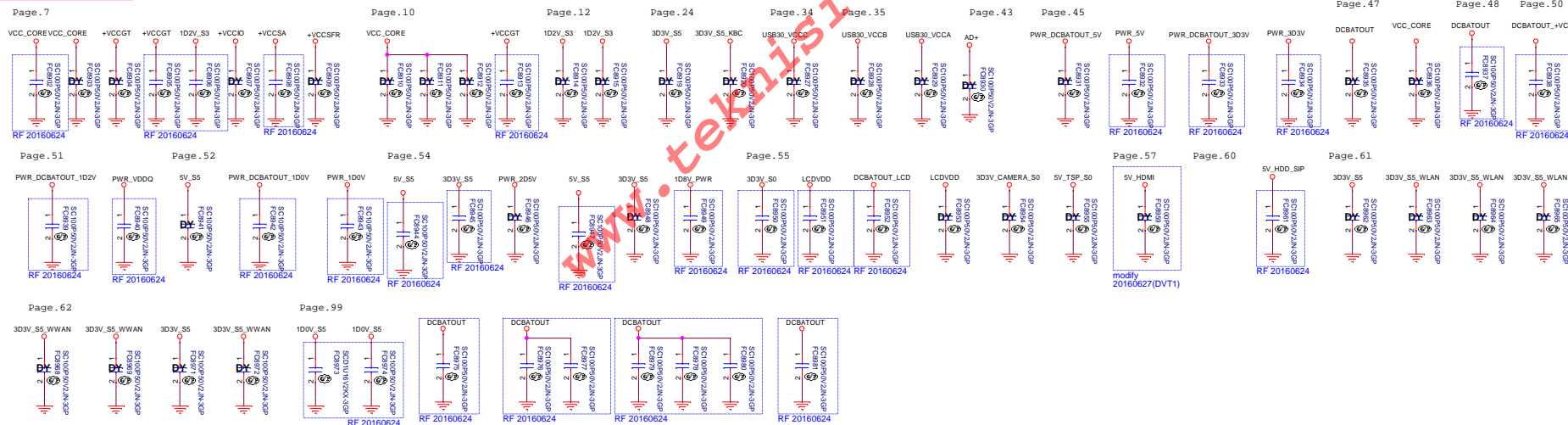
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
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remove PAD5,PAD6..20160603


change PAD1 from ZZ.00PAD.J11 to ZZ.00PAD.V71..20160623



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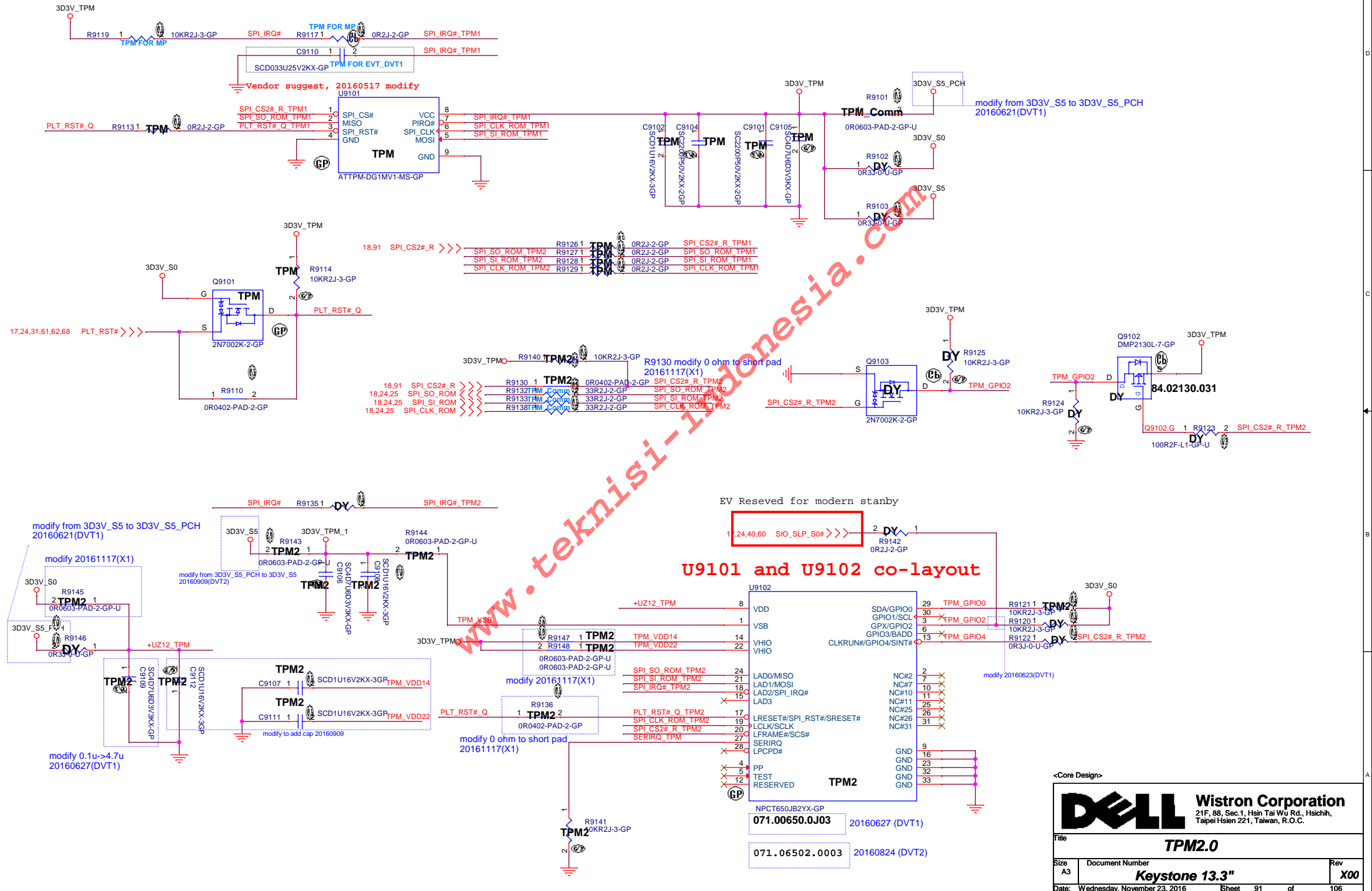
Title

Reserved

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SSID = TPM



<Core Design>

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Title **TPM2.0**

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Title
(Reserved)Finger Print


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Title

(Reserved)

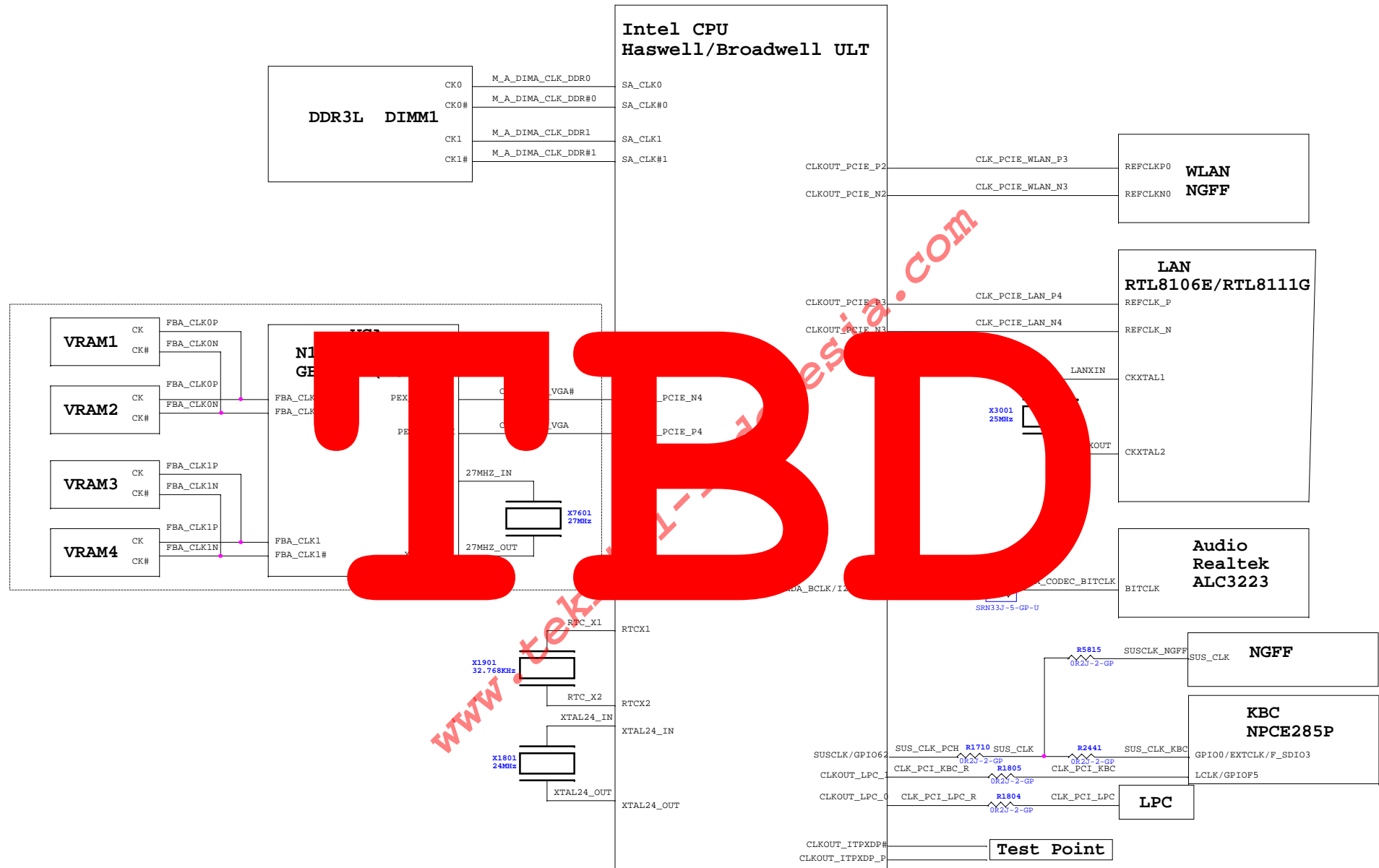
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CLK Block Diagram

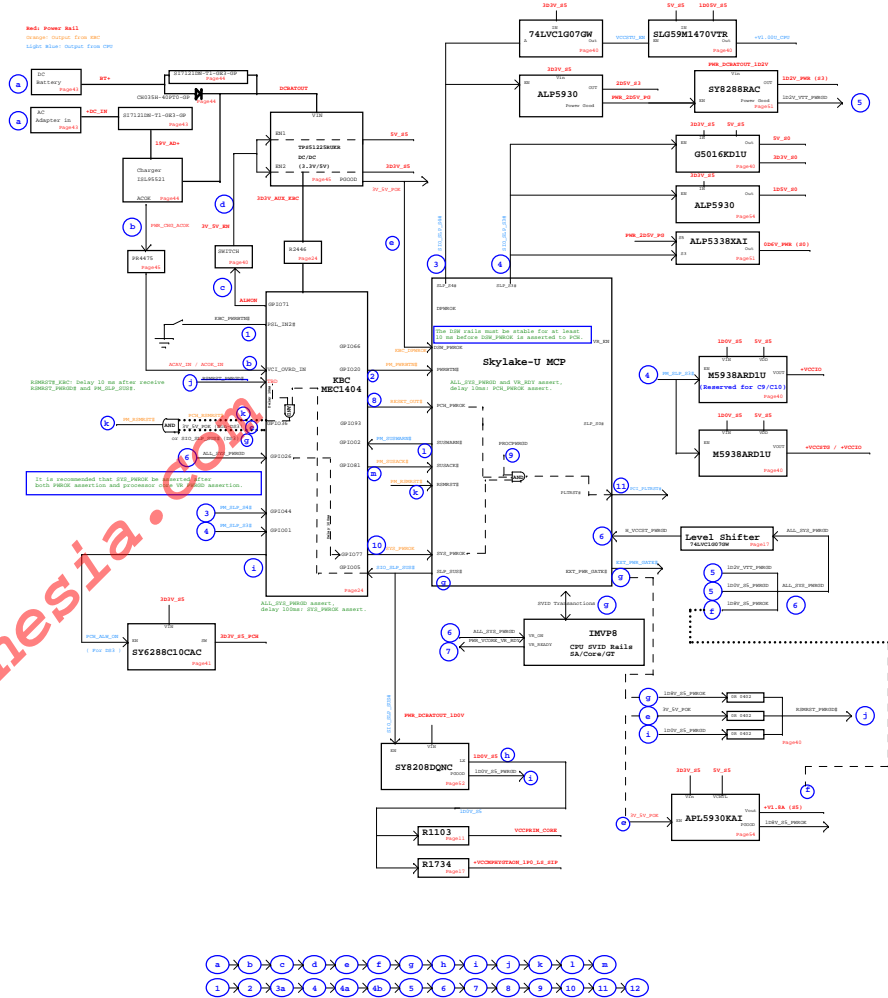


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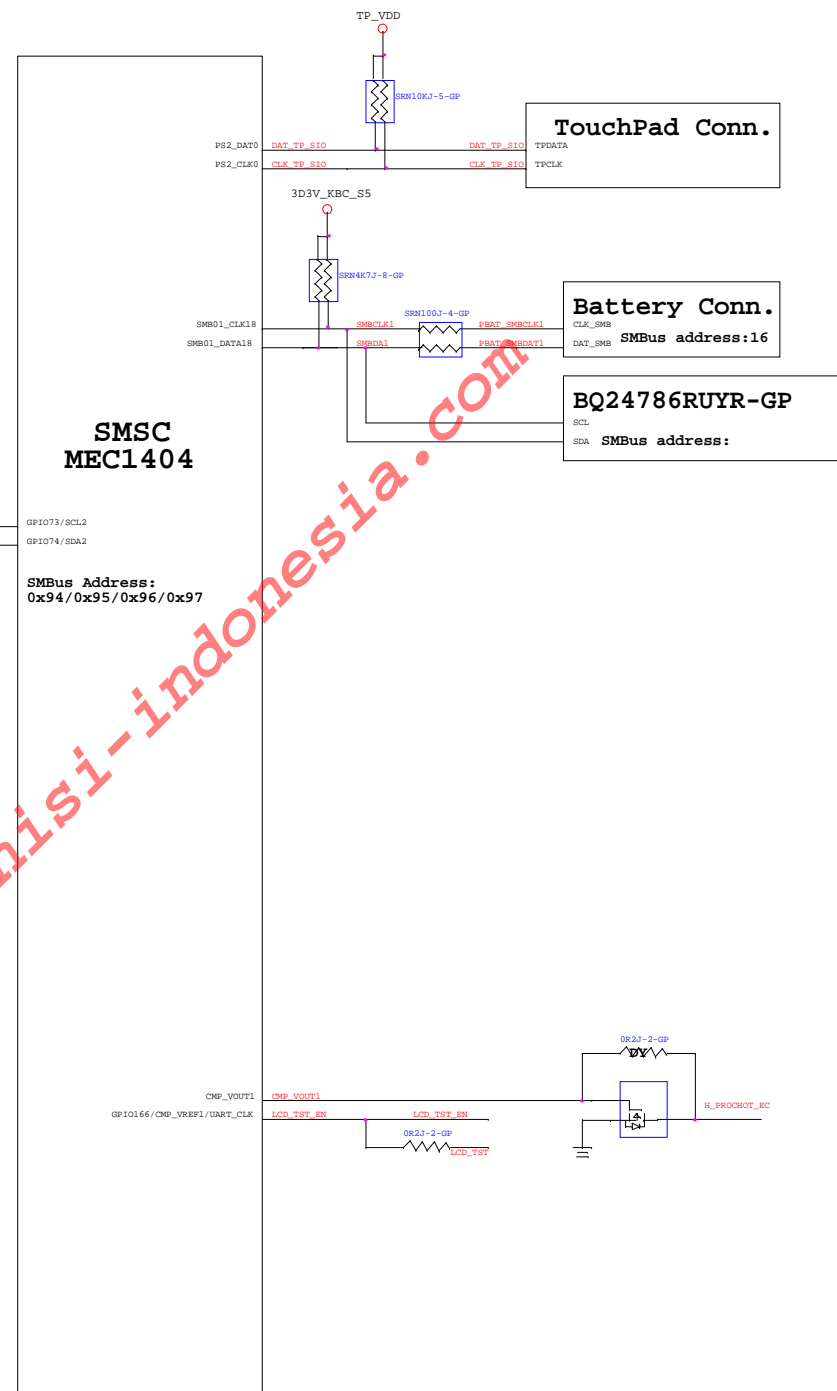
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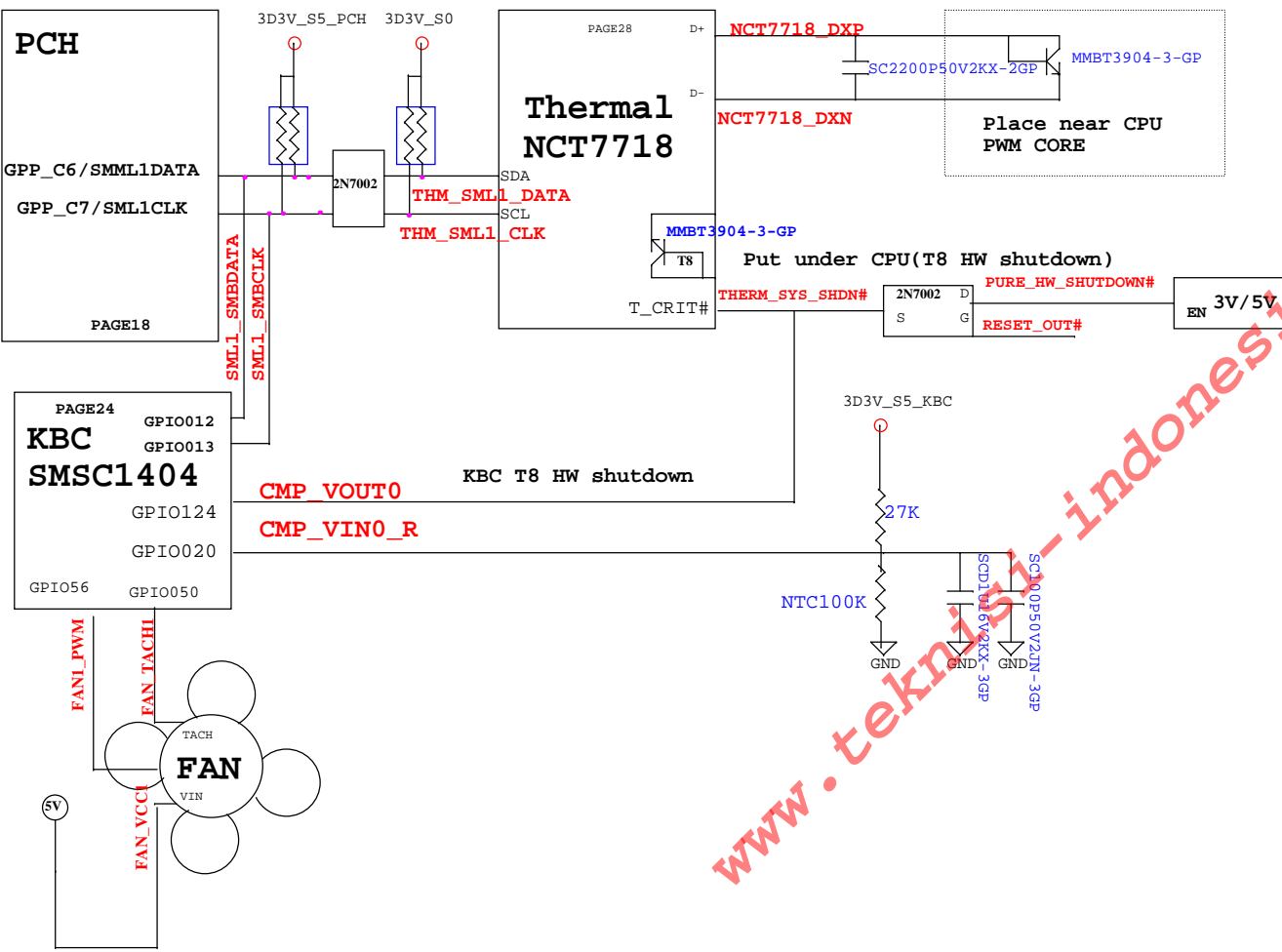
The timing diagram shows three digital signals over time. The signals are labeled 2D5V_S3, 1D2V_S3, and 0D6V_S0. The signals are high for a period and then transition to low. The transition for 2D5V_S3 occurs first, followed by 1D2V_S3, and then 0D6V_S0.



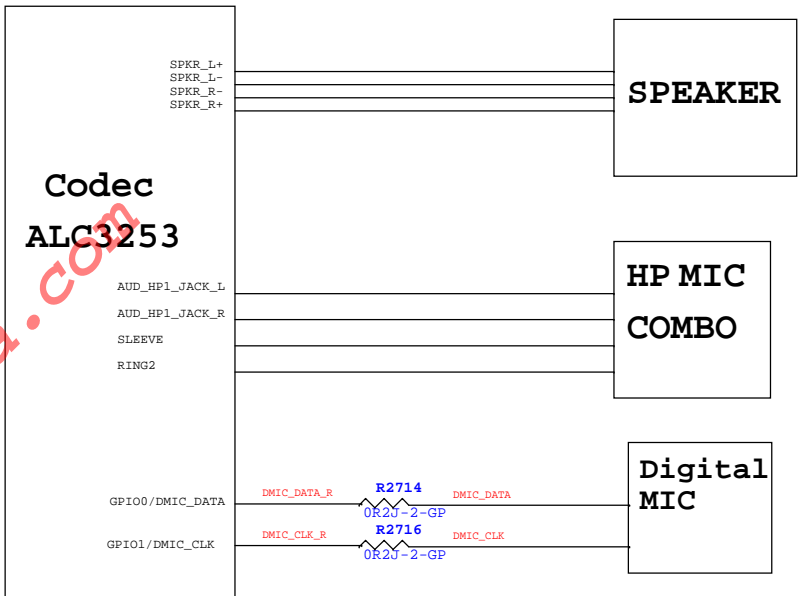
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



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SIP connector

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